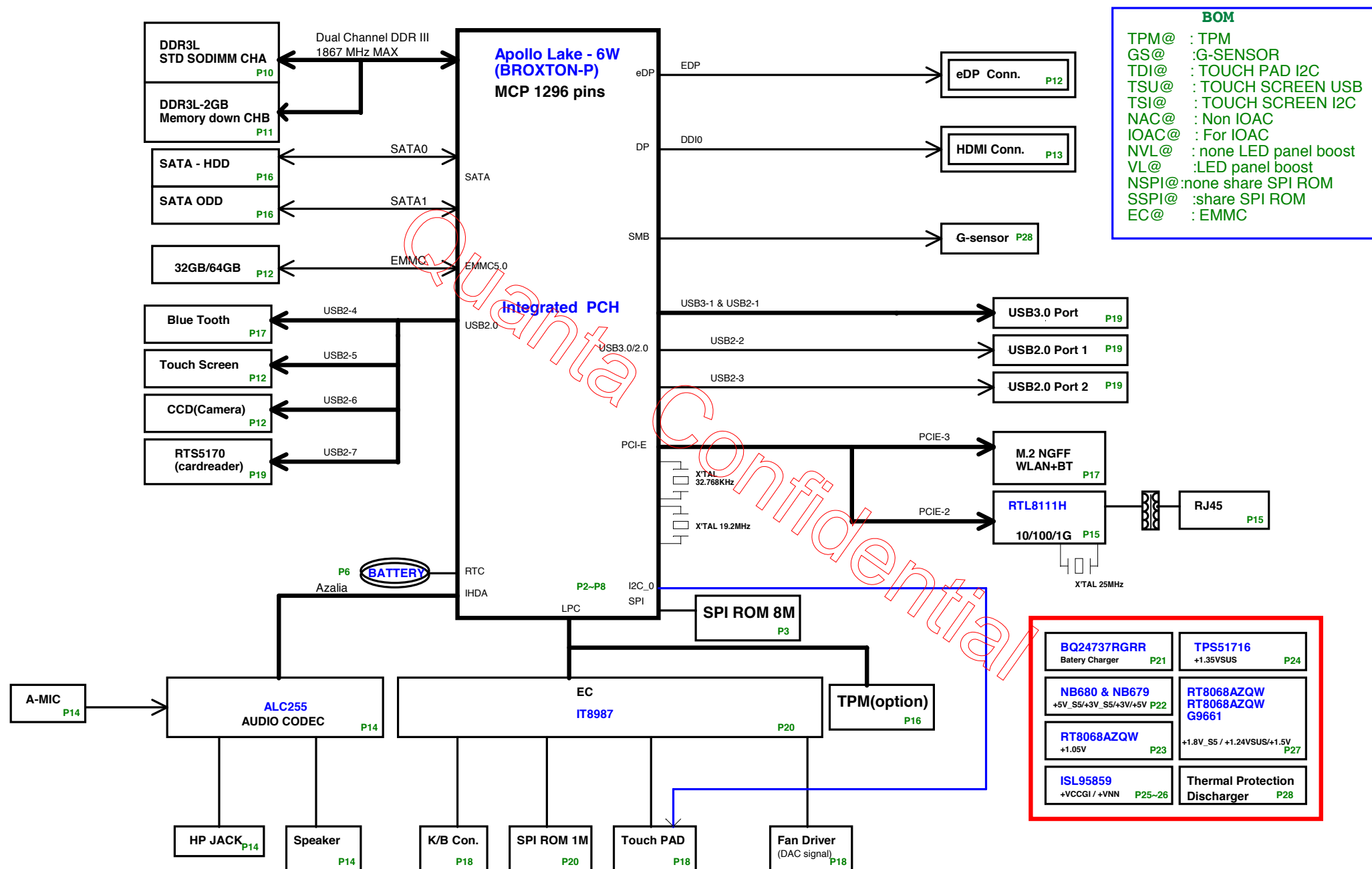
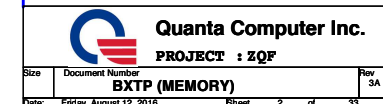
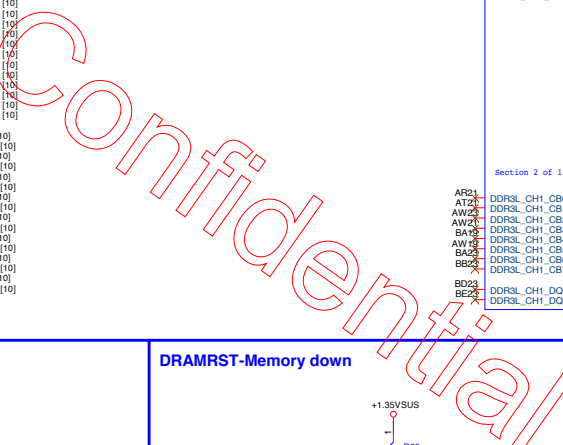
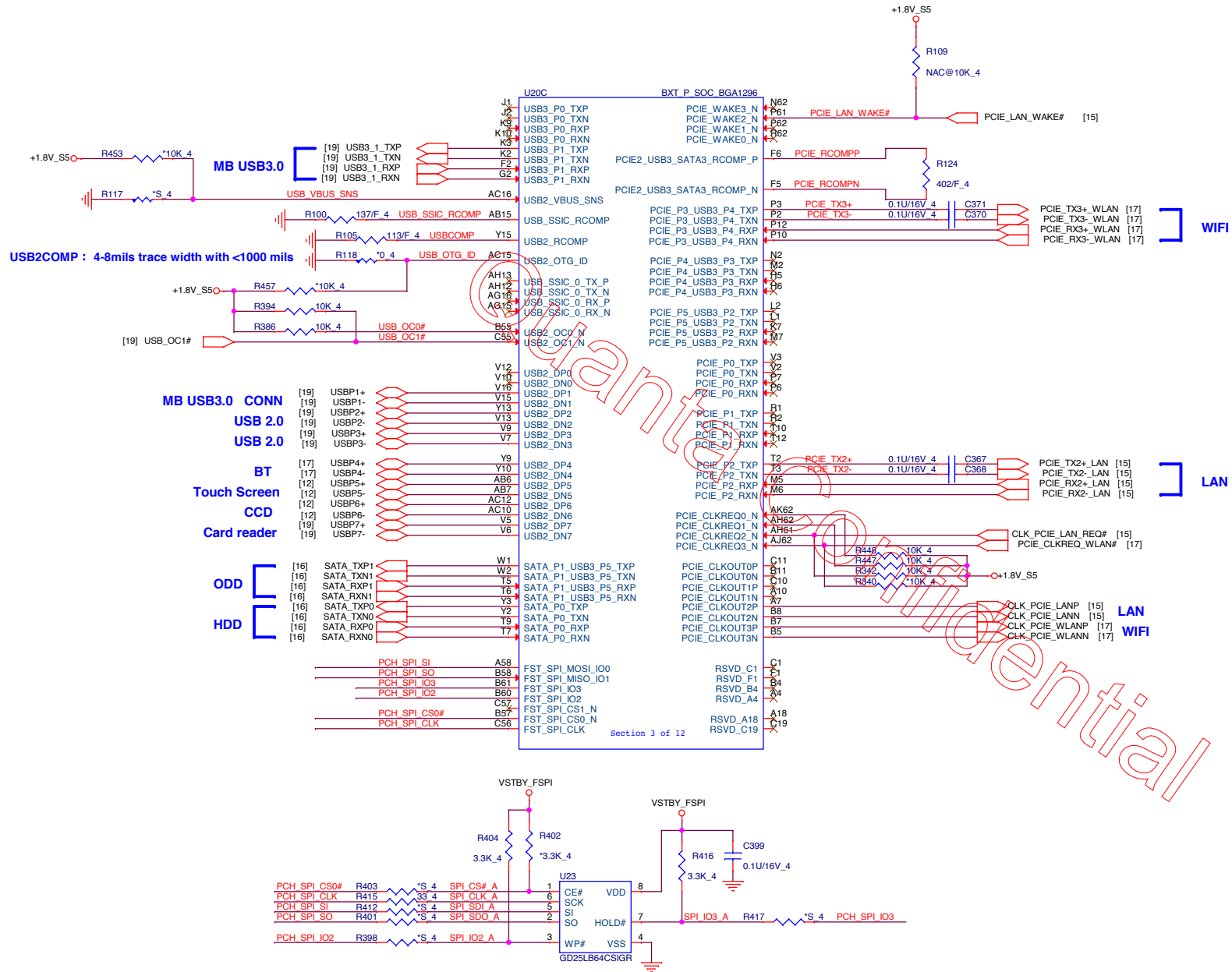


ZQF SYSTEM BLOCK DIAGRAM



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SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
1.8V	WND	8M	AKE5EZN0N01	W25Q64FWSSIQ
	GGD	8M	AKE5EG-0Q01	GD25LB64CSIGR

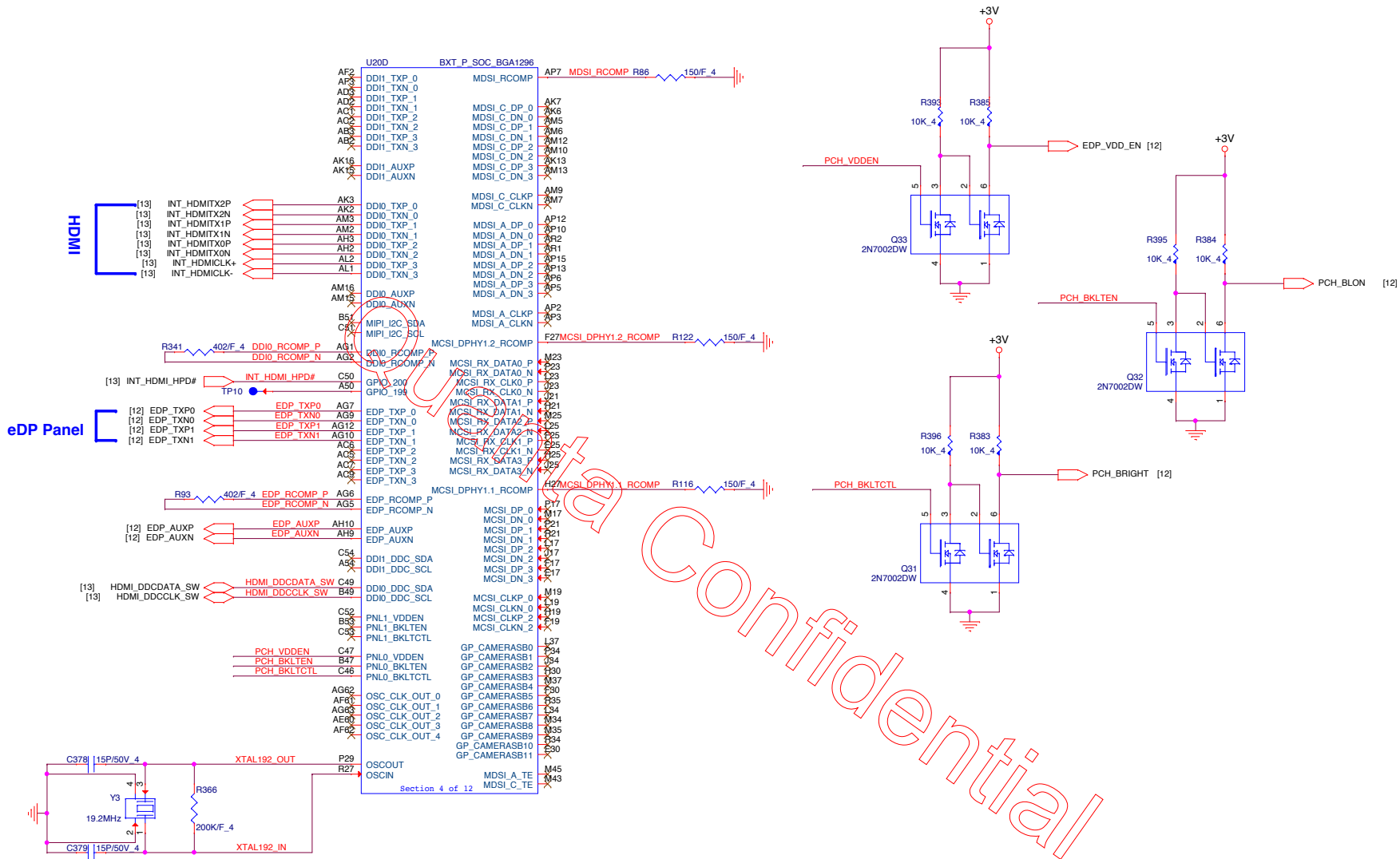
Quanta Computer Inc.

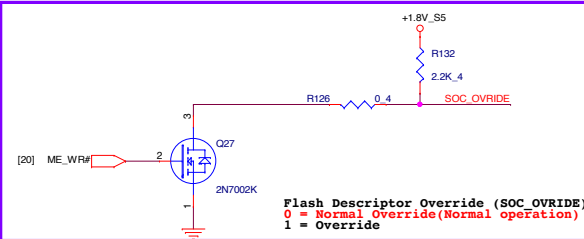
PROJECT : ZQF

BXTP (PCIE/USB/SATA/SPI)


Size: Document Number: Rev: 3A

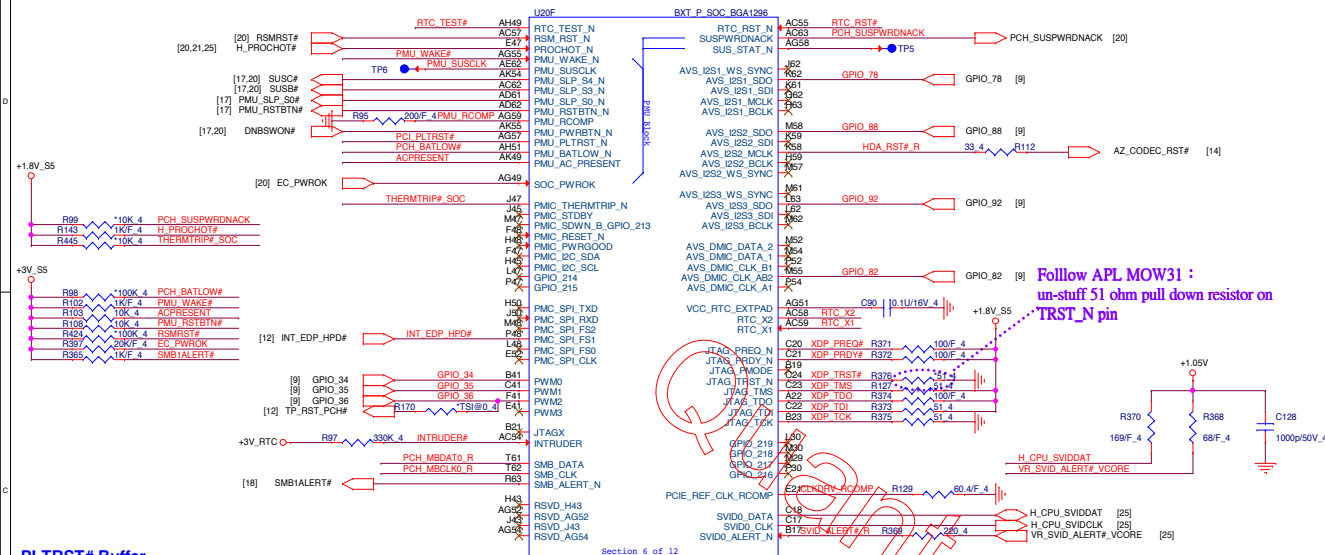
Date: Friday, August 12, 2016 Sheet: 3 of 33



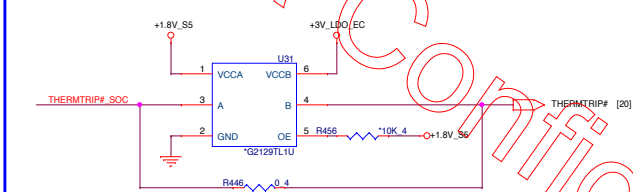


<u>RAM_ID3</u>	<u>RAM_ID2</u>	<u>RAM_ID1</u>	<u>RAM_ID0</u>	Vender	Quanta PN	Description
0	0	0	0	Samsung-2GB	AKD5JG0T504	IC SDRAM(96P)K4B4G1646E-BYKO(FPGA)STNBSQ
0	0	0	1	Hynix-2GB	AKD5PG8TW13	IC SDRAM(96P)H5TC46K3CPR-PBA(FPGA)STNBSQ
0	0	1	0	Miron-2GB	AKD59GSTL12	IC SDRAM(96P)MT41K256M16TW-107:P STNBSQ

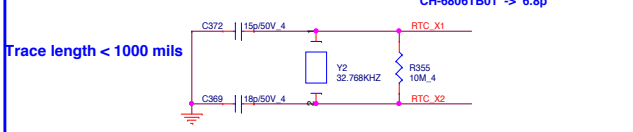
 Quanta Computer Inc. PROJECT : ZQF	
Size	Document Number
BXTP (EMMC/LPC/SMB/ISH)	
Date:	Friday, August 12, 2016
	Sheet 5 of 33



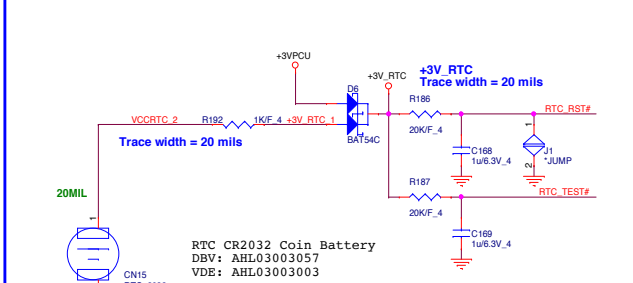
THERMALTRIP#



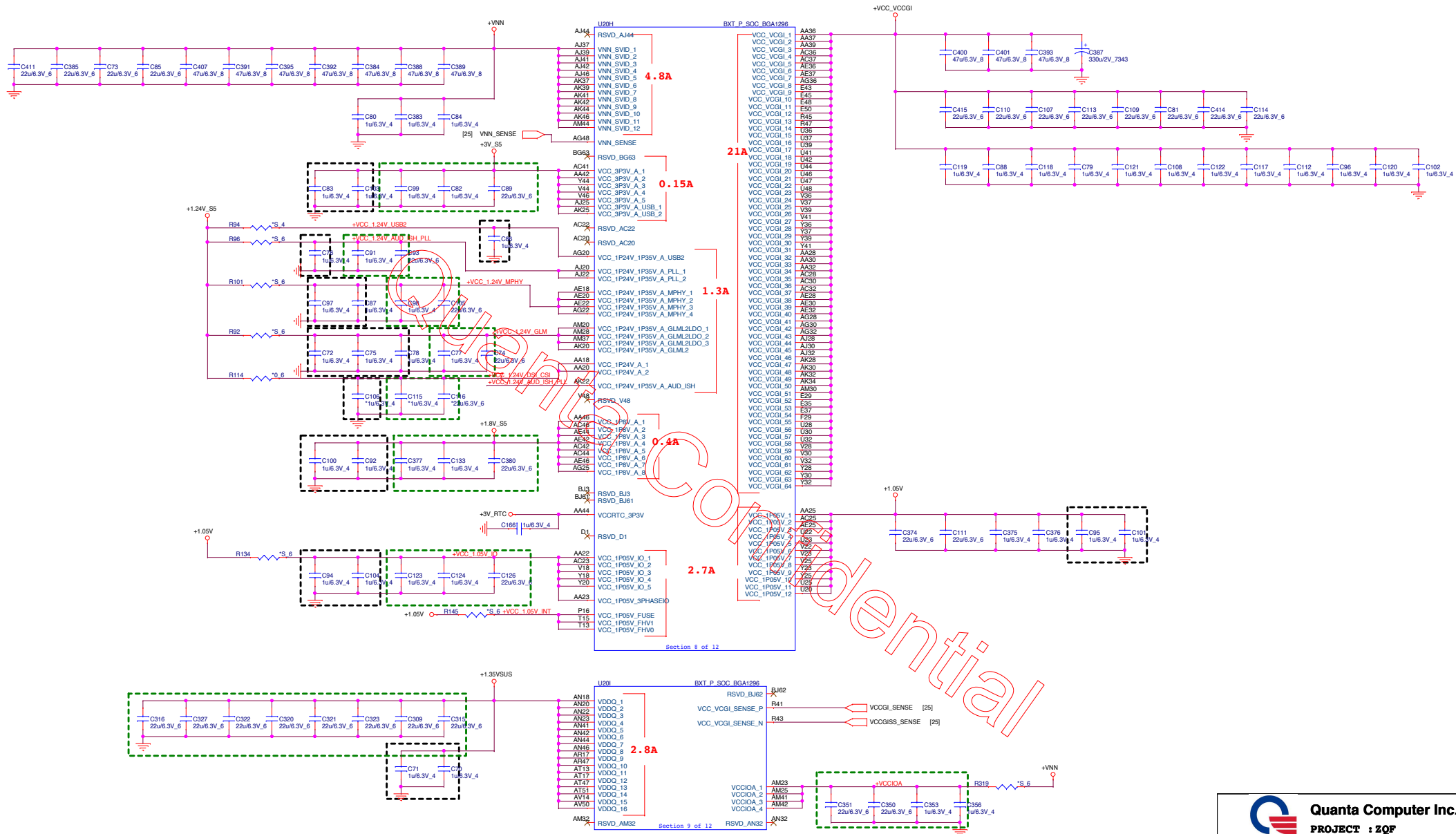
RTC Clock 32.768KHz (CPU)



RTC Circuitry (RTC)

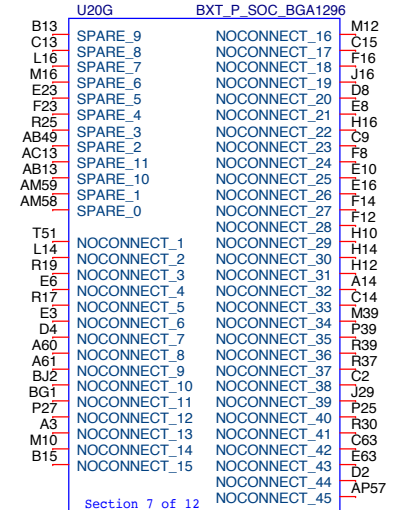
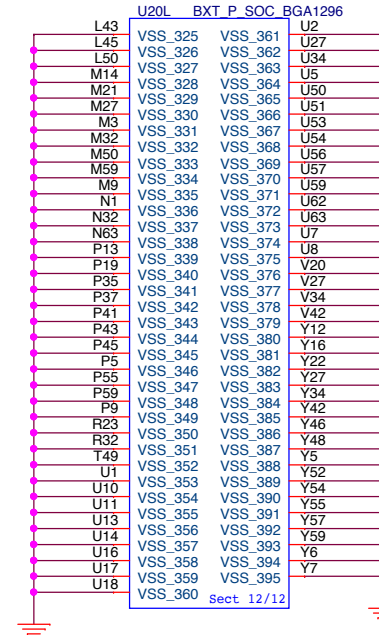
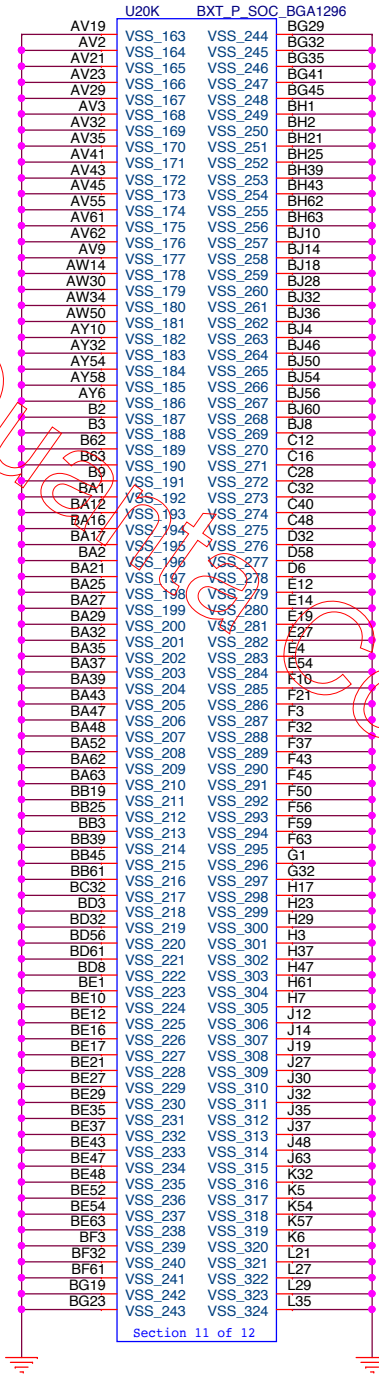
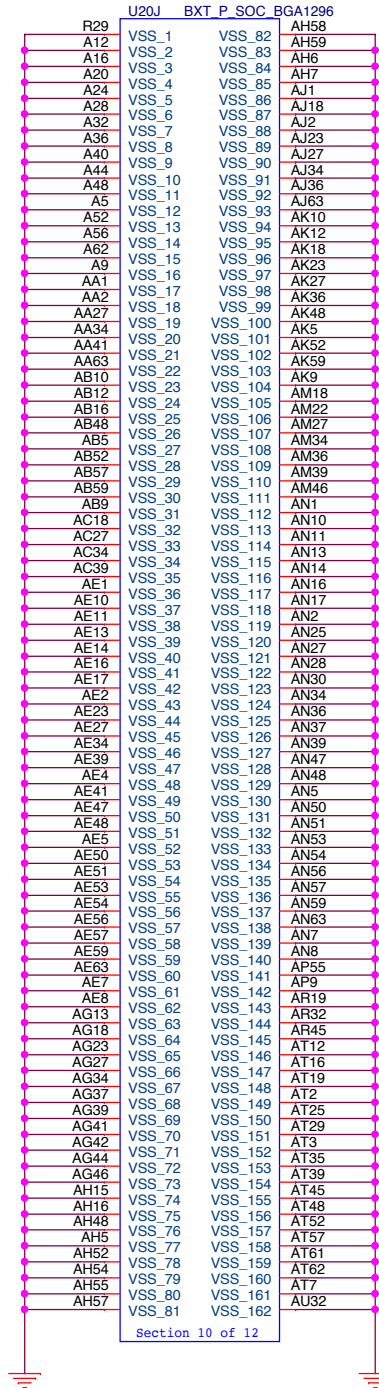


Apollolake (POWER)

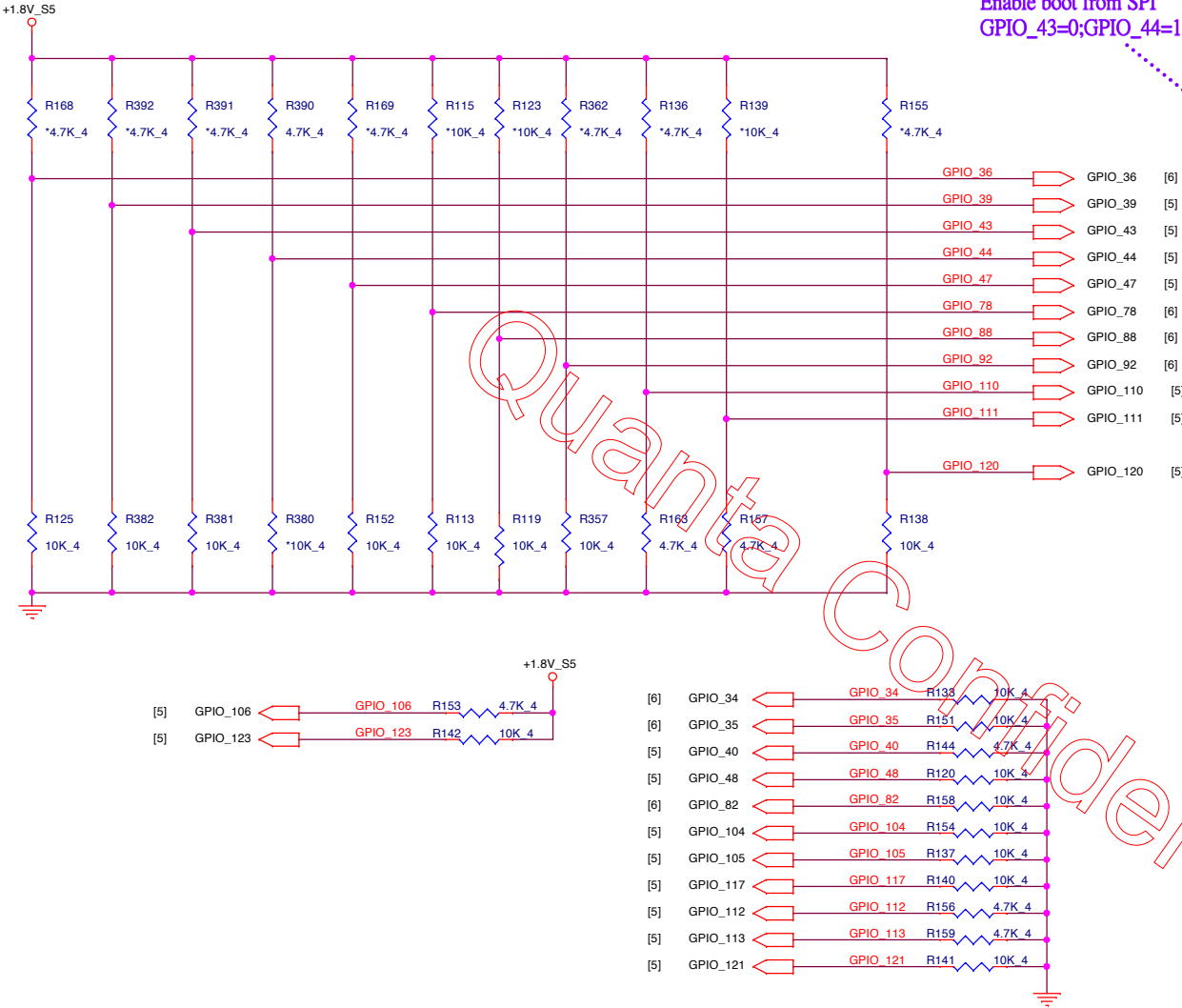


Apollolake ULT (GND)

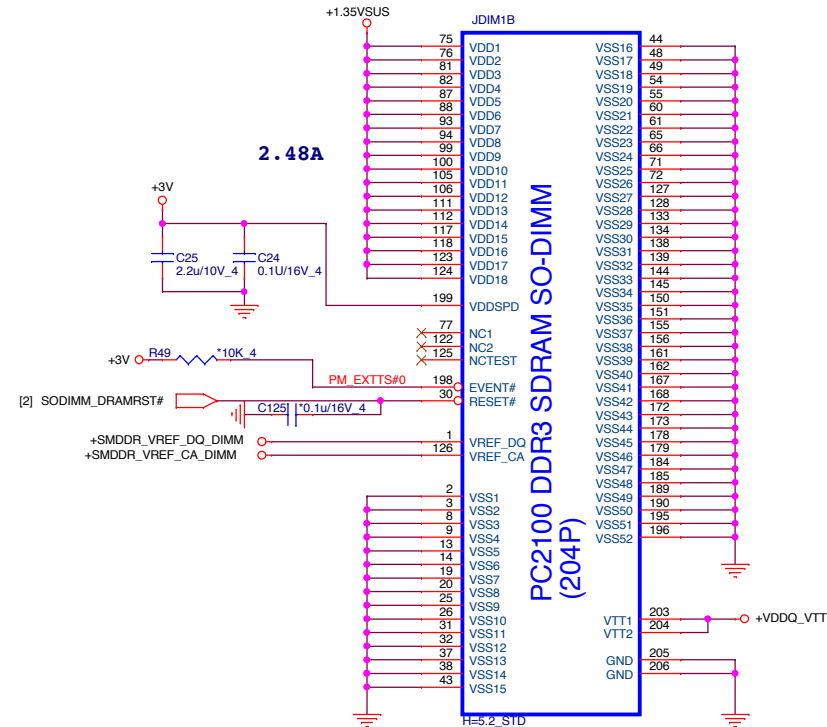
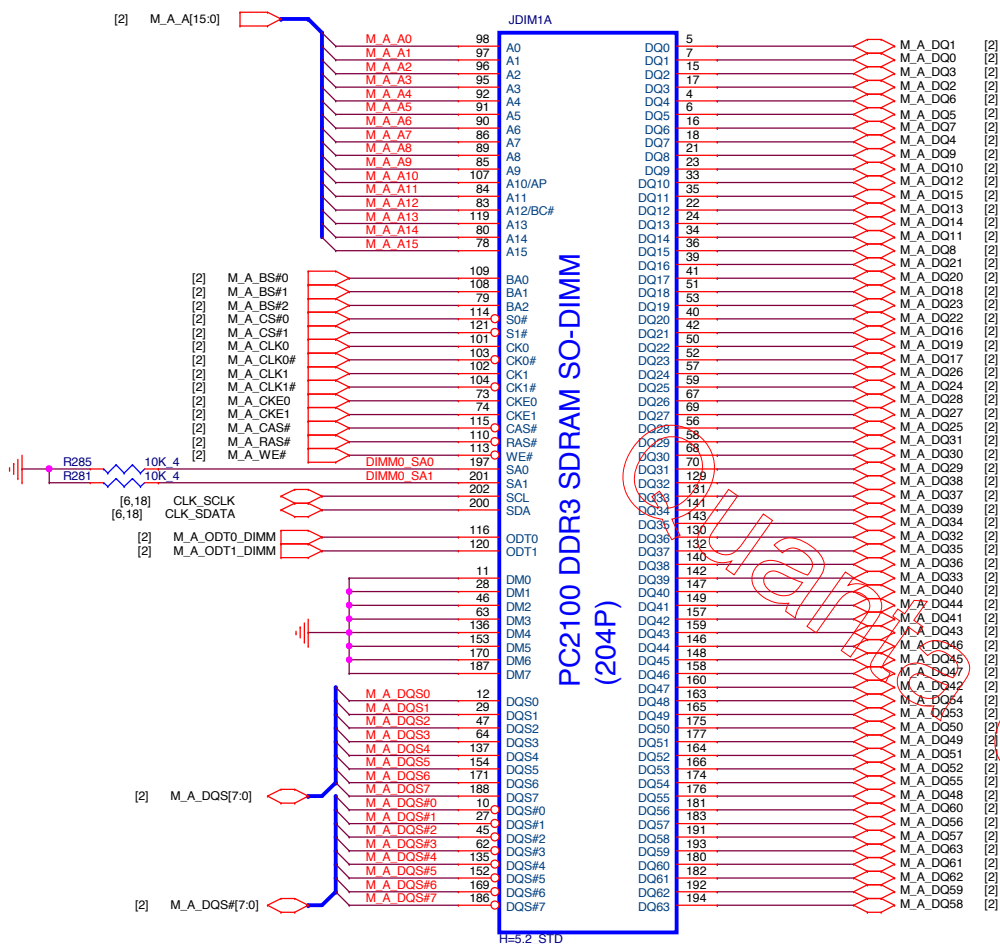
08



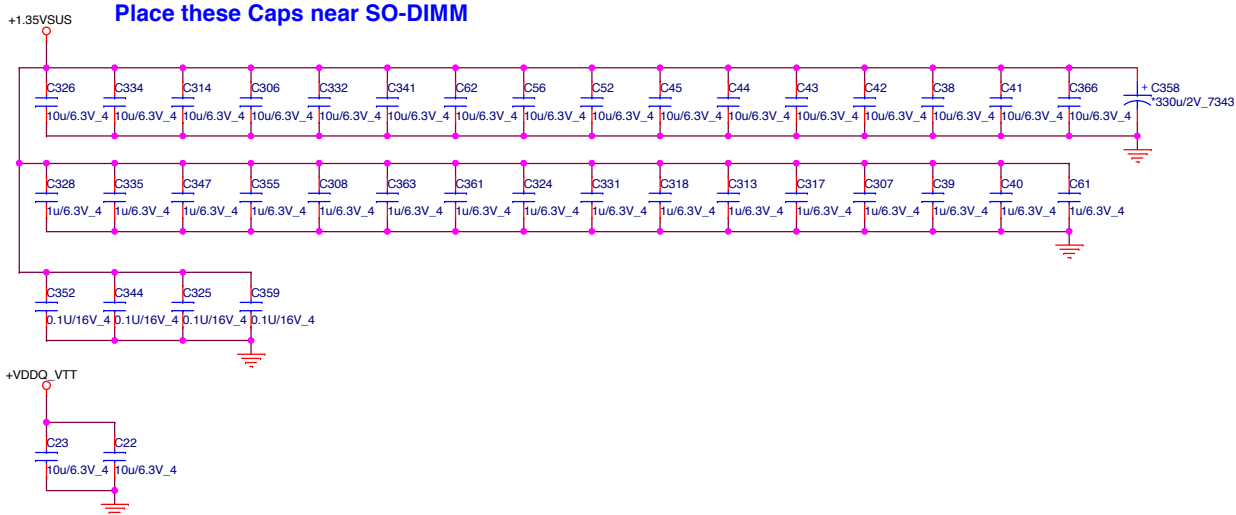
HARDWARE STRAPS



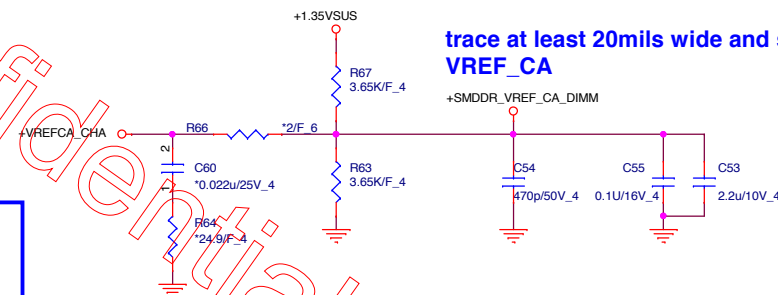
Hardware Strap	Strap Description
GPIO_36	VCC_1P24V_1P35V_A voltage select 0 = 1.24V 1 = 1.35V
GPIO_39	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass
GPIO_43	Allow eMMC as a boot source 0 = Disable 1 = Enable
GPIO_44	Allow SPI as a boot source 0 = Disable 1 = Enable
GPIO_47	Force DNX FW Load 0 = Do not force 1 = Force
GPIO_78	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V
GPIO_88	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_92	SMBus No Re-Boot 0 = Disable (default) 1 = Enable
GPIO_110	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_111	Boot BIOS Strap 0 = Boot from SPI 1 = Do not boot from SPI
GPIO_120	Top swap override 0 = Disable 1 = Enable



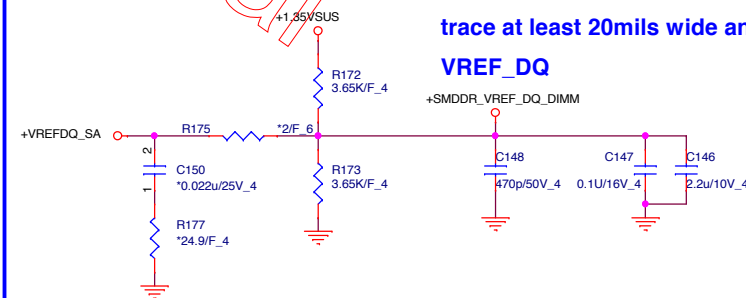
Place these Caps near SO-DIMM



trace at least 20mils wide and space VREF_CA



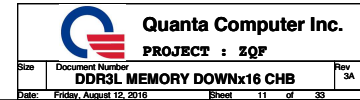
trace at least 20mils wide and space VREF_DQ



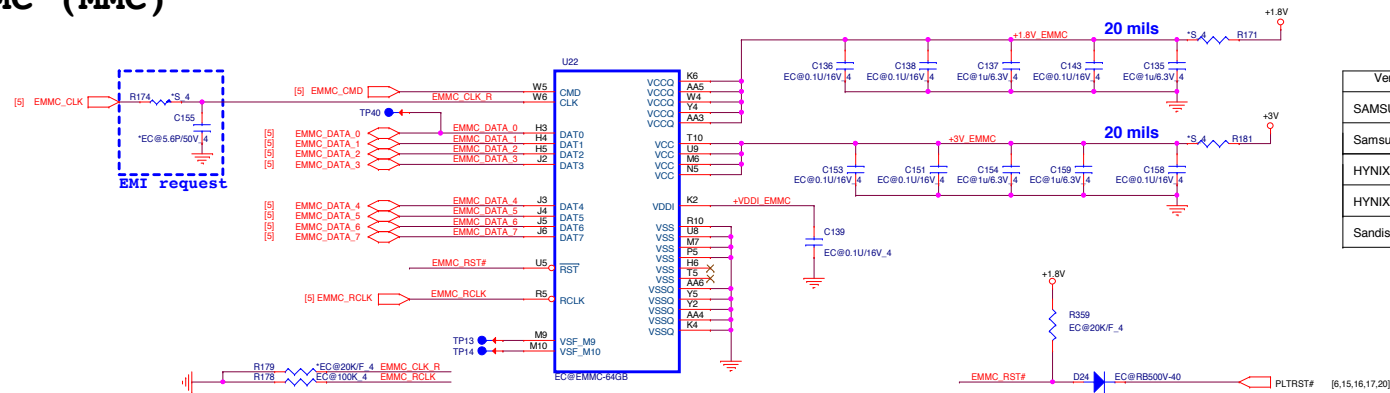
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PROJECT : ZQF

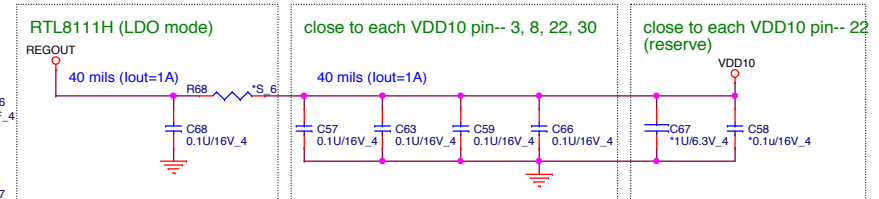
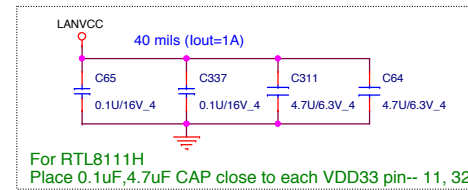
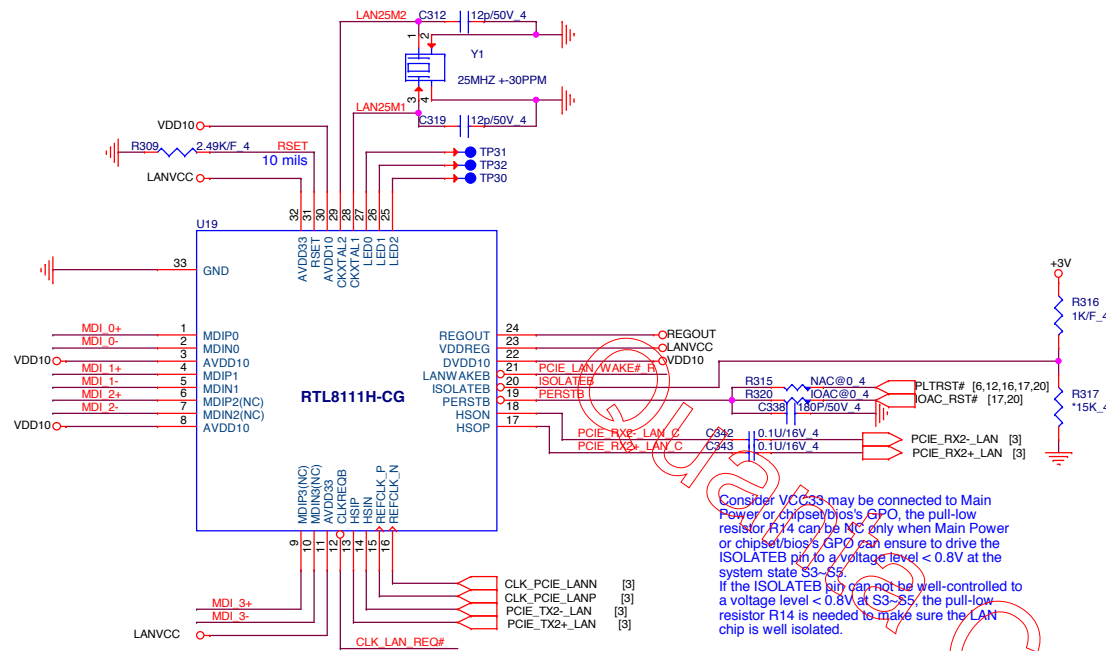
Size	Document Number	Rev
	DDR3L SODIMM-STD CHA	3A
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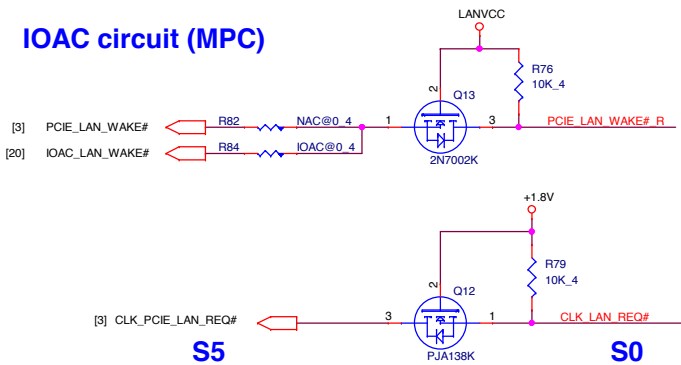
eMMC (MMC)



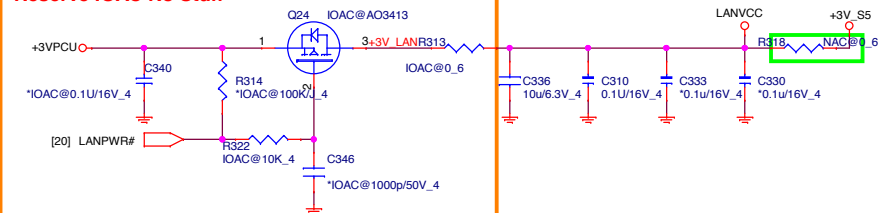
Size	Document Number	Rev
	HDM/Hall sensor	3A
Date:	Friday, August 12, 2016	Sheet 13 of 33



IOAC circuit (MPC)

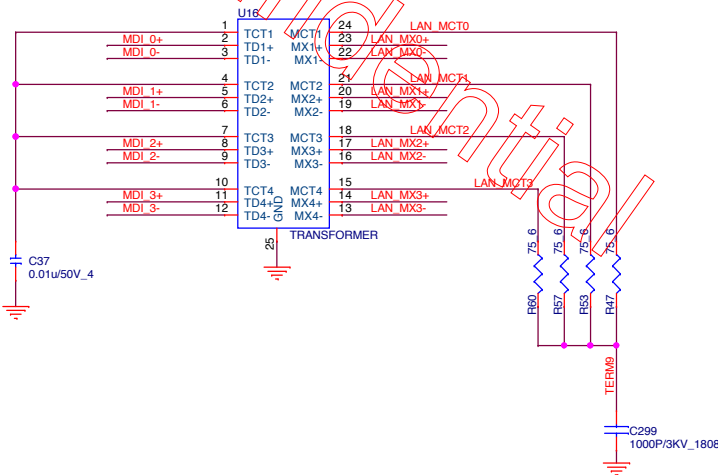


Reserve IOAC No Stuff

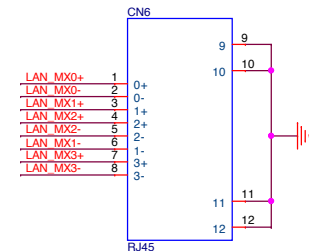


Transformer

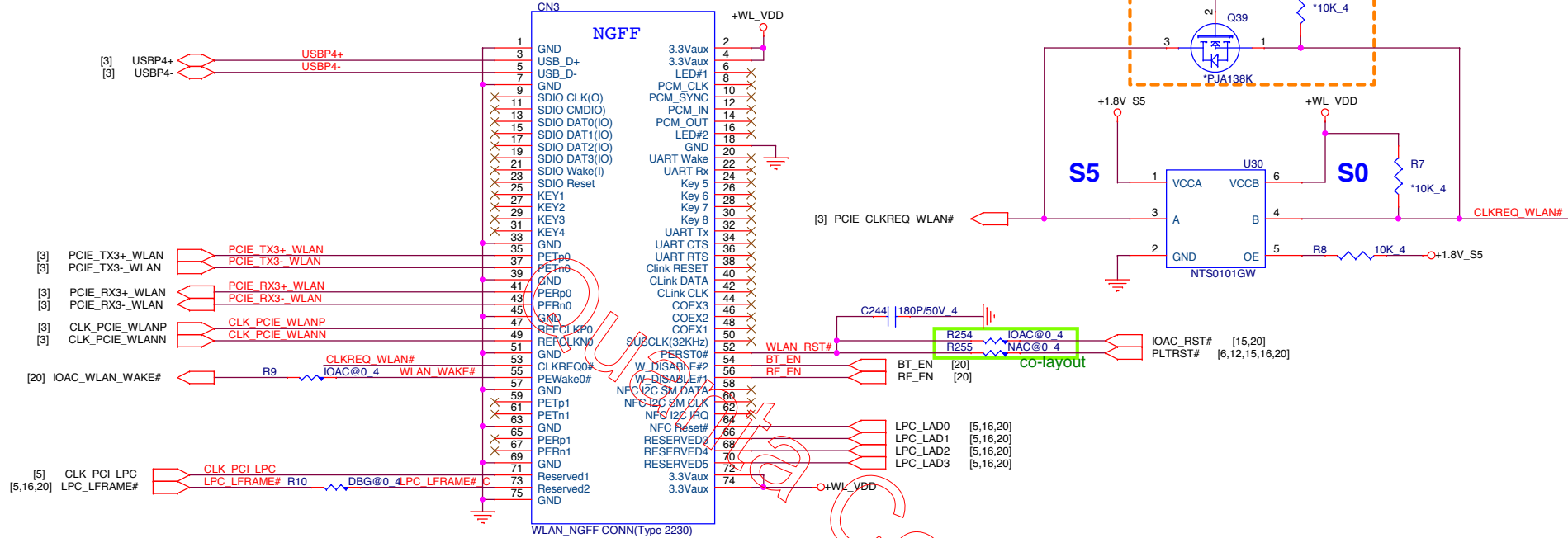
Layout: All termination signal should have 30 mil trace



RJ45 Connector

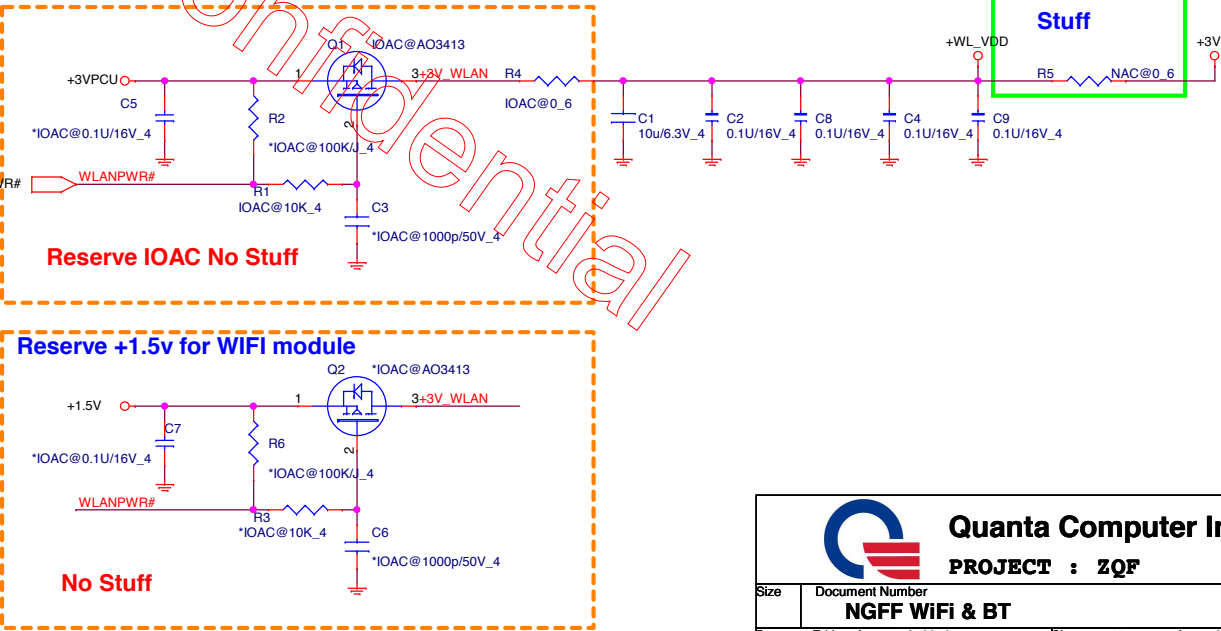


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PROJECT : ZQF

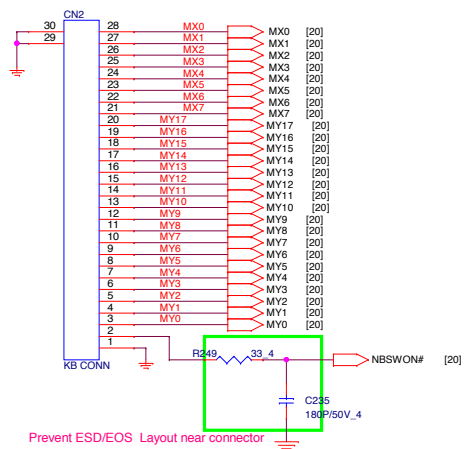


Low	Mini card +3V power enable
High	Mini card +3V power disable

Intel APS Fixture use

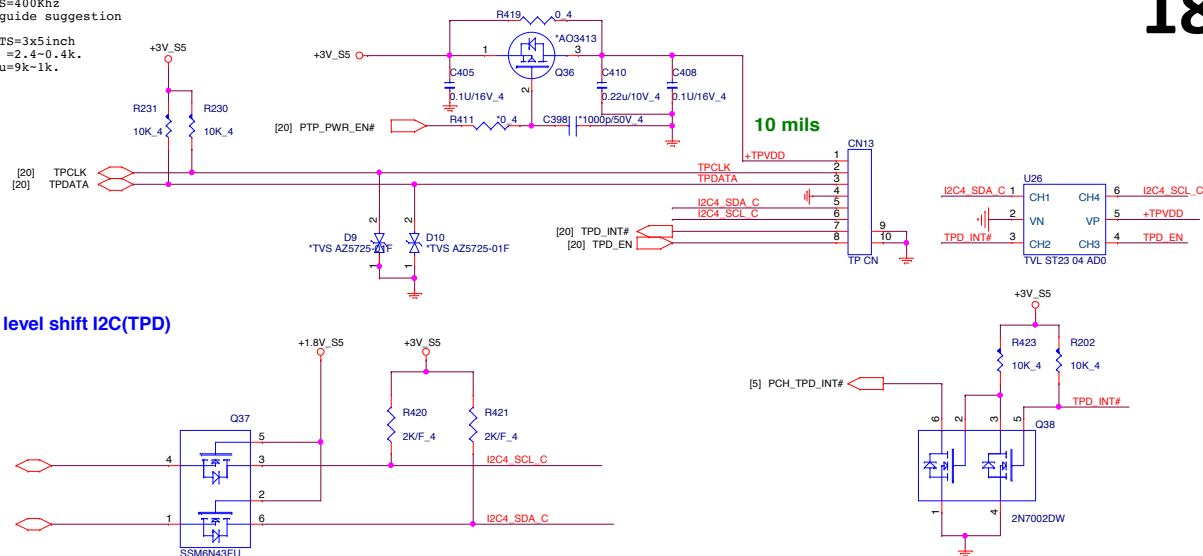


KEYBOARD (KBC)

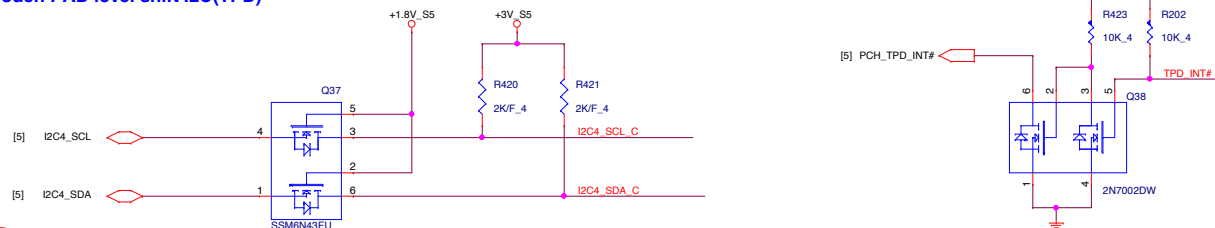


TOUCHPAD BOARD ONTP (TPD I2C/PS2 co-lay)

TPD->100KHz, TS=400KHz
Intel design guide suggestion
NCP Pin 10u.
Per inch 3u TS=3x5inch
400KHz10-100u = 2.4-0.4k.
100KHz 10-100u=9k-1k.

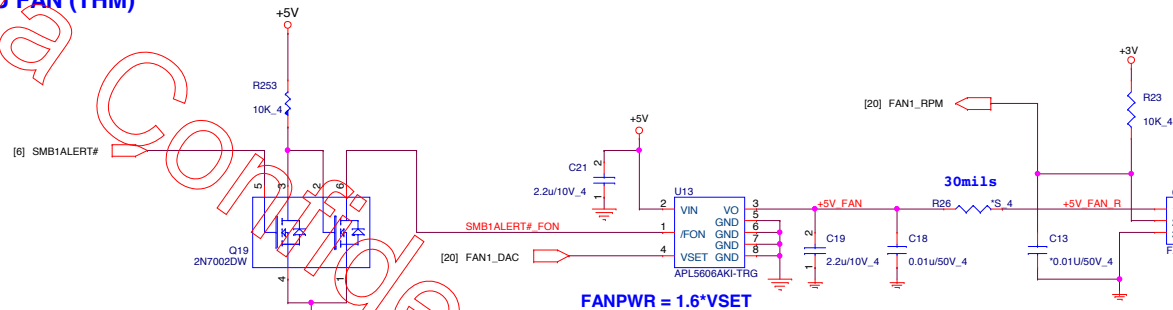


Touch PAD level shift I2C(TPD)

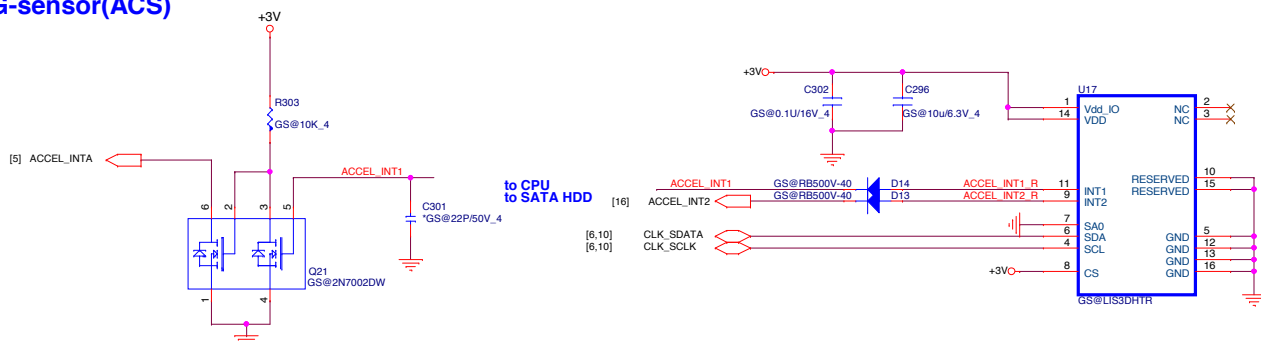


KB_BL LED (KBC)

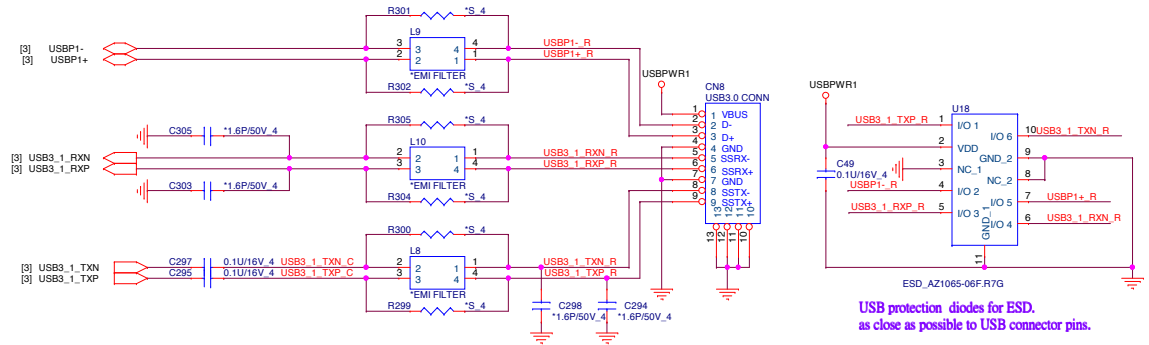
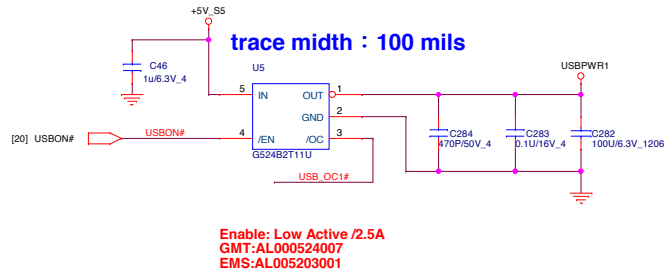
CPU FAN (THM)



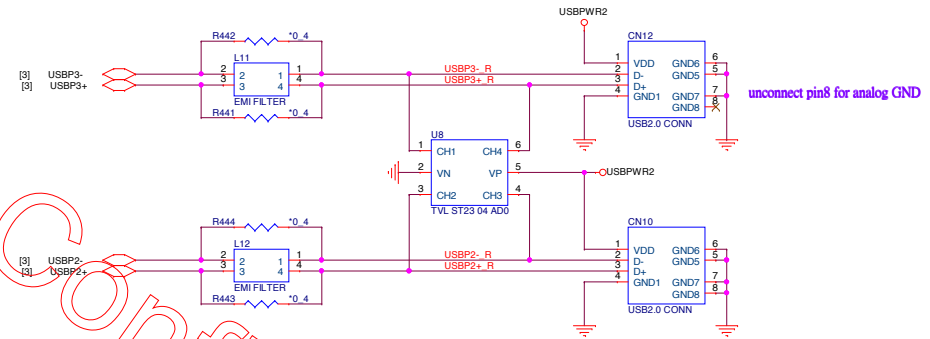
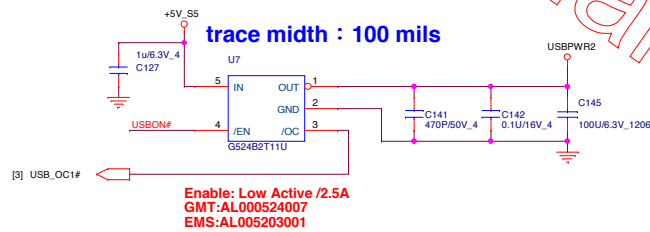
G-sensor(ACS)



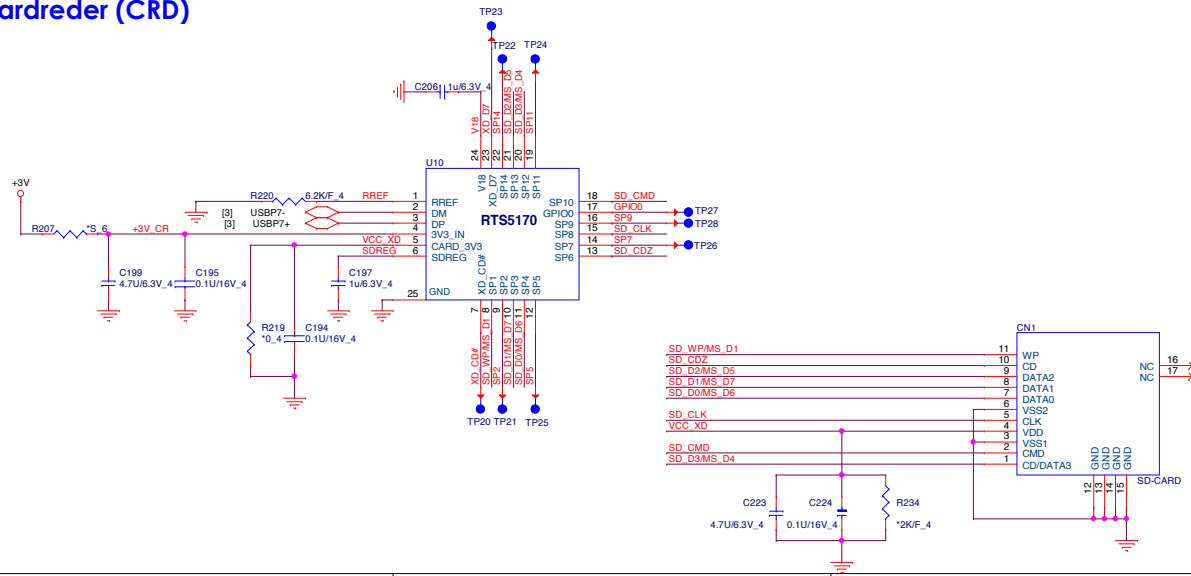
USB 3.0 Connector (UB3)



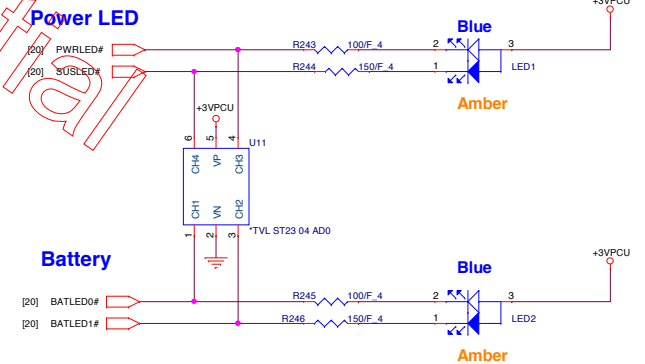
USB 2.0 Connector (UB2)

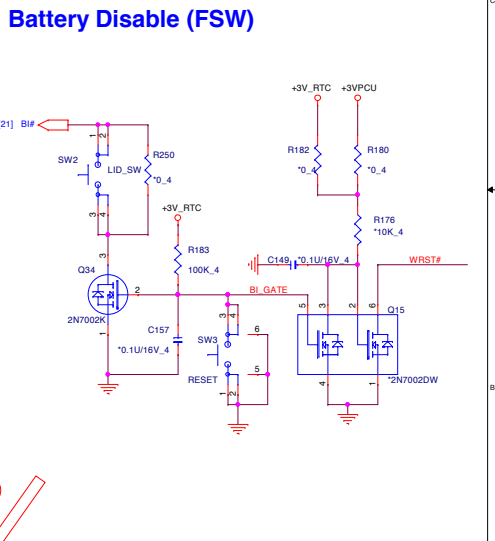
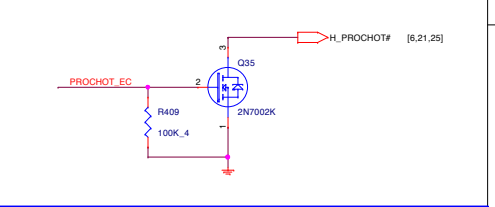
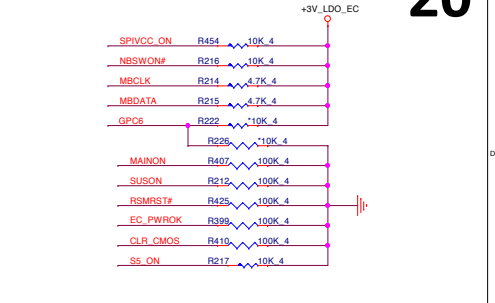
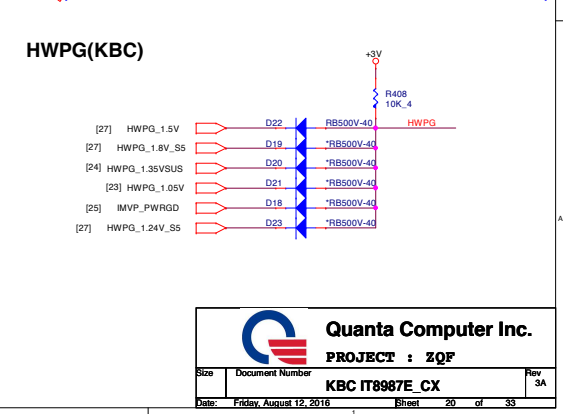
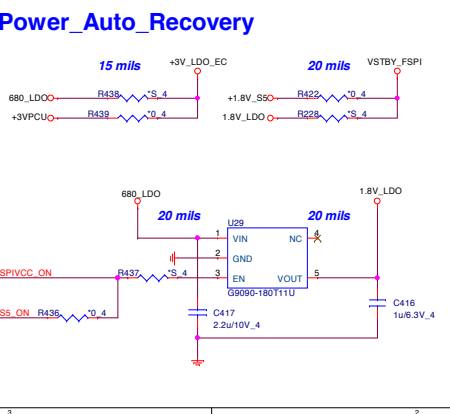
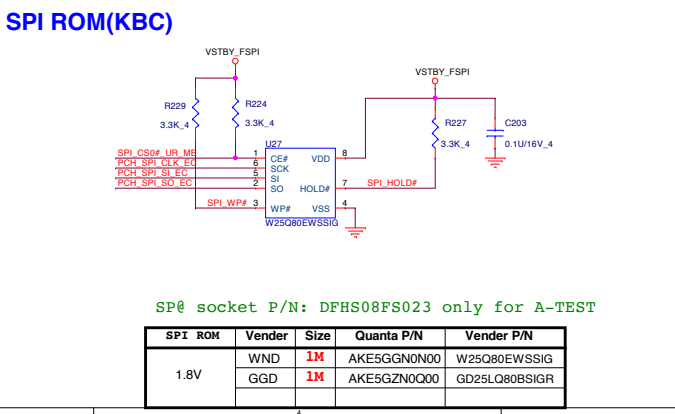
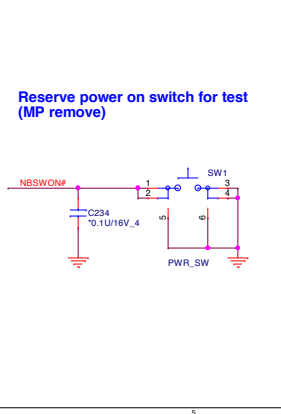
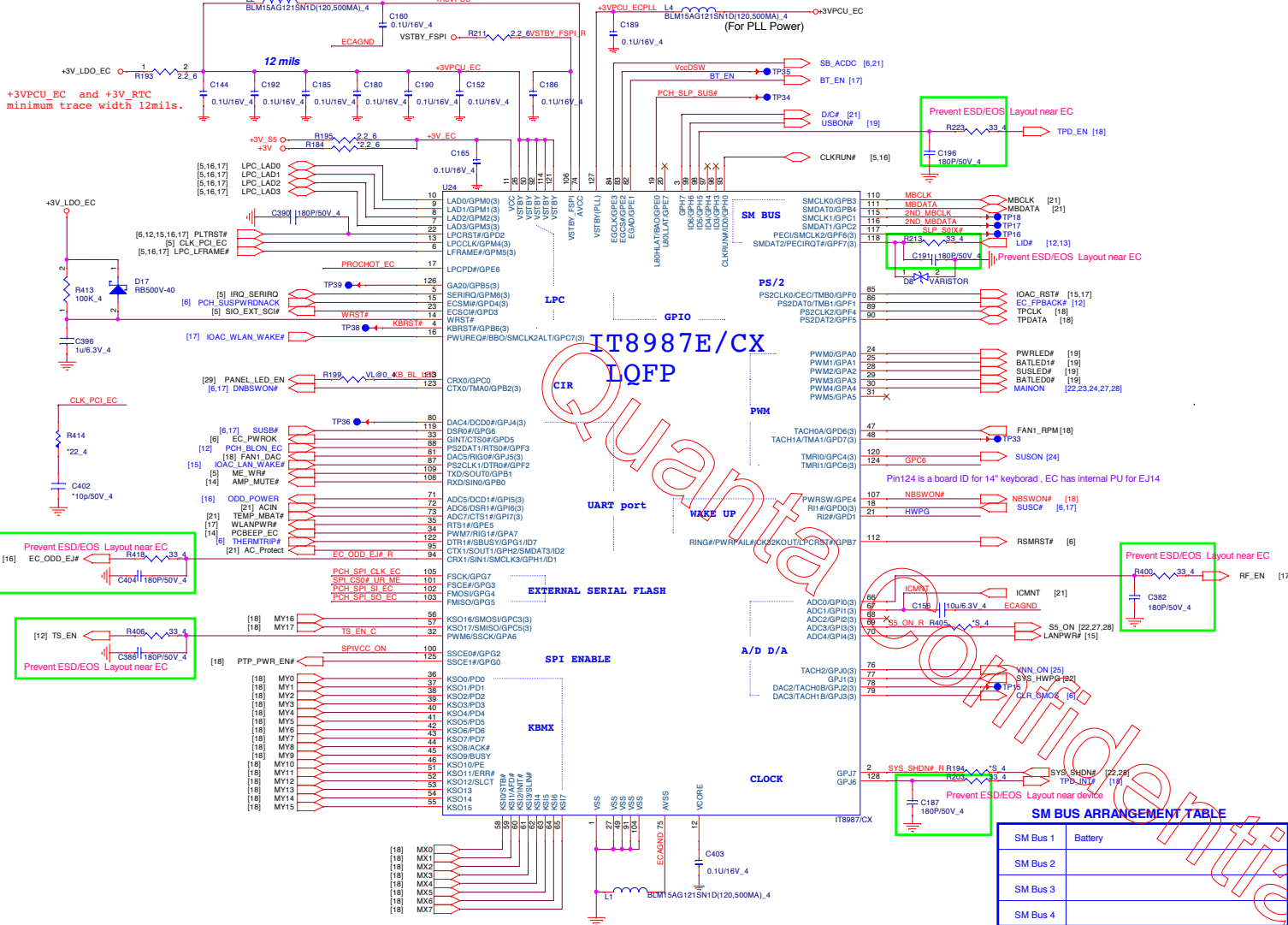


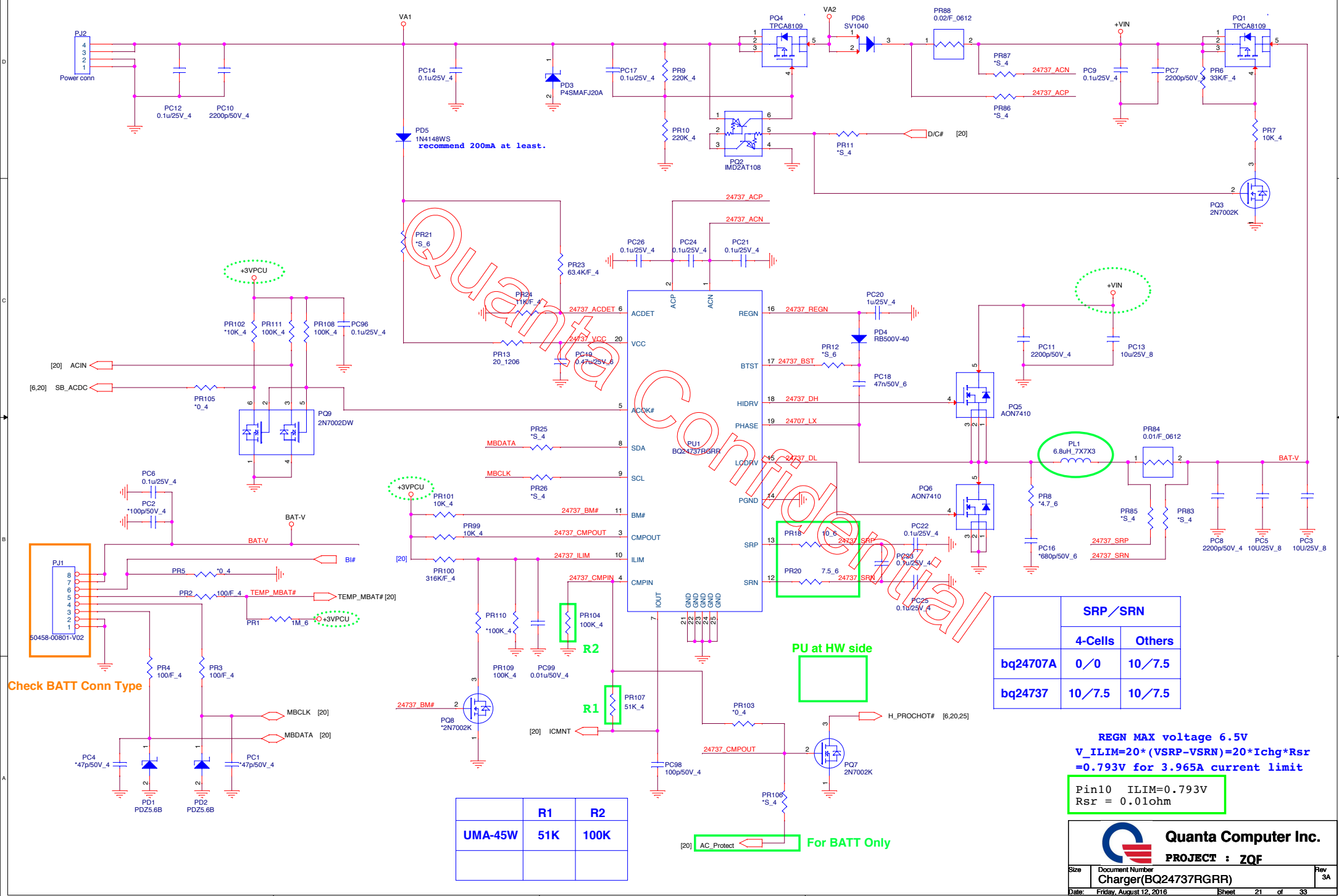
Cardreader (CRD)

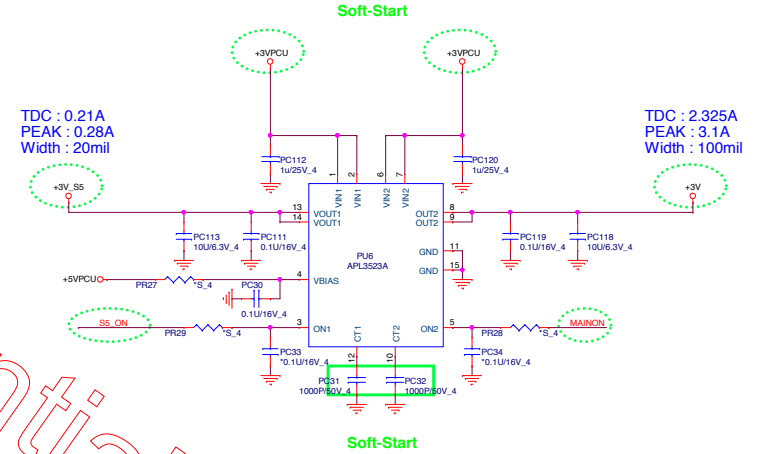
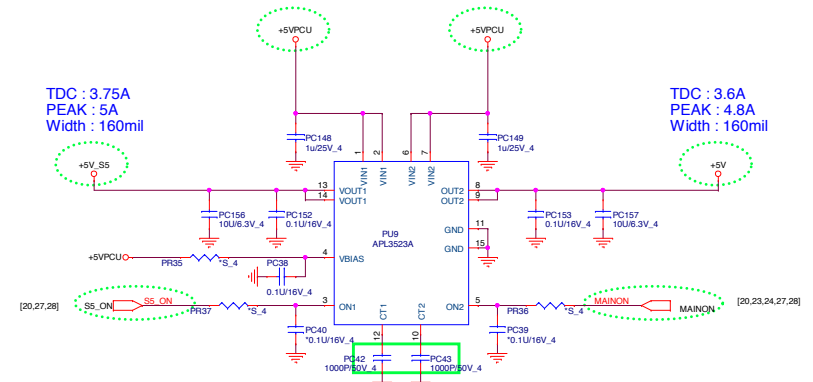
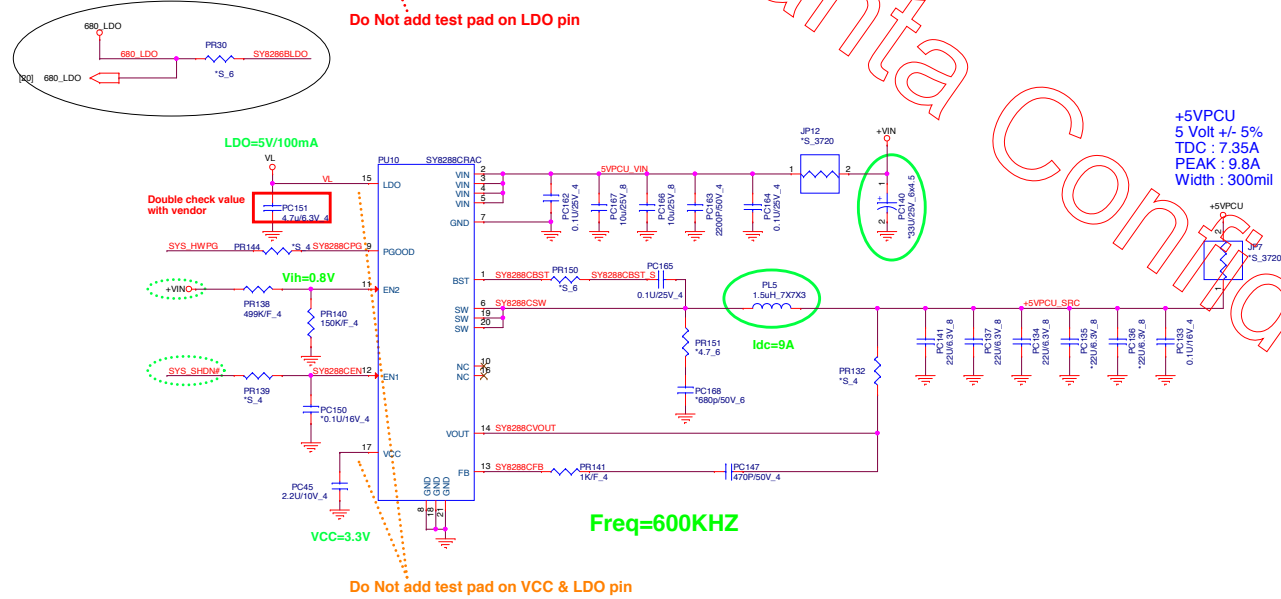
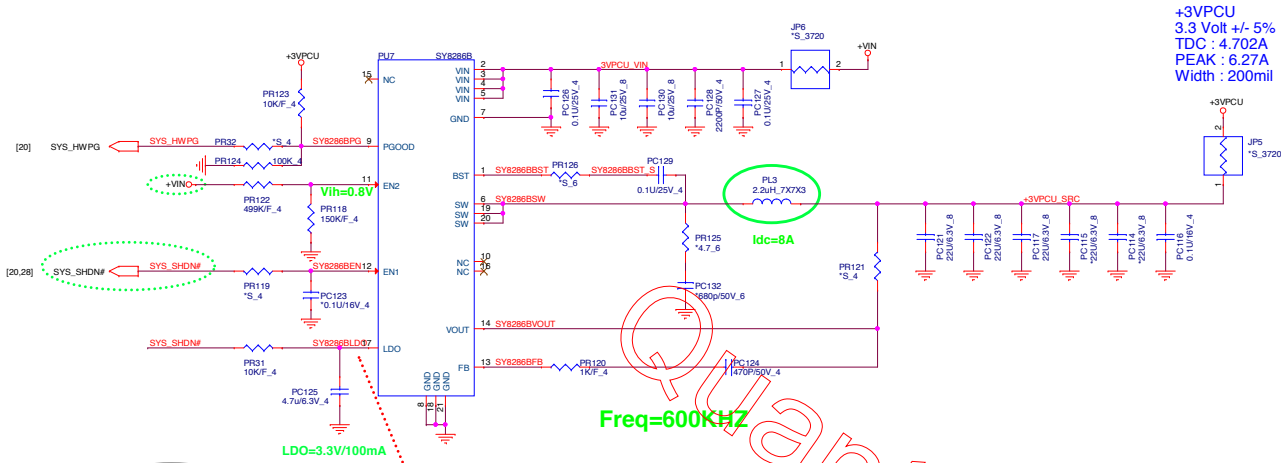


LED(UIF)

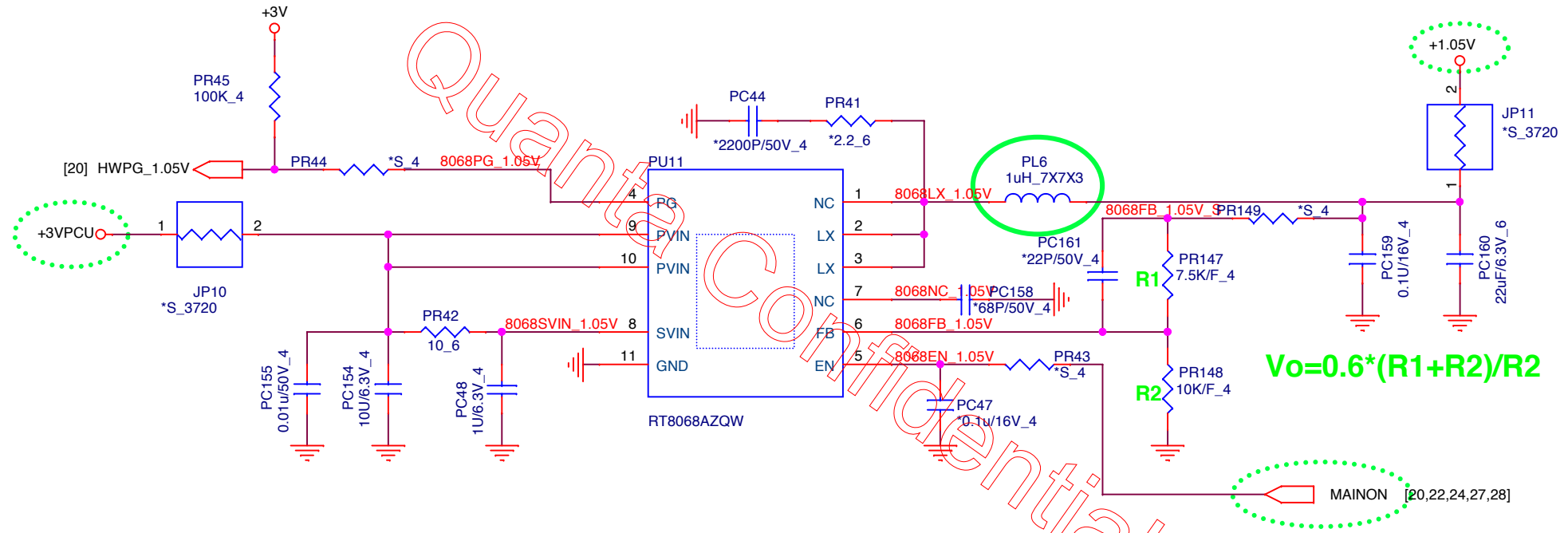








+1.05V
 1.05Volt +/- 5%
 TDC : 2.025A
 PEAK : 2.7A
 Width : 100mil



$$Vo=0.6*(R1+R2)/R2$$

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PROJECT :

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	+1.05V (RT8068AZQW)	3A
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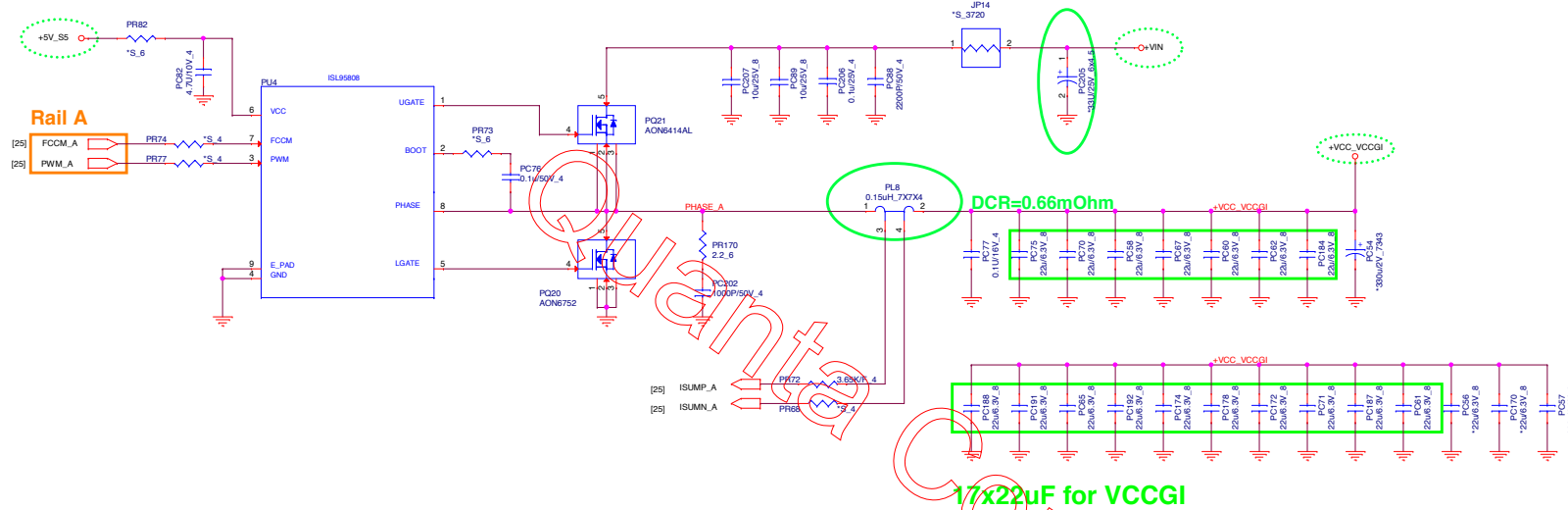
PROJECT :

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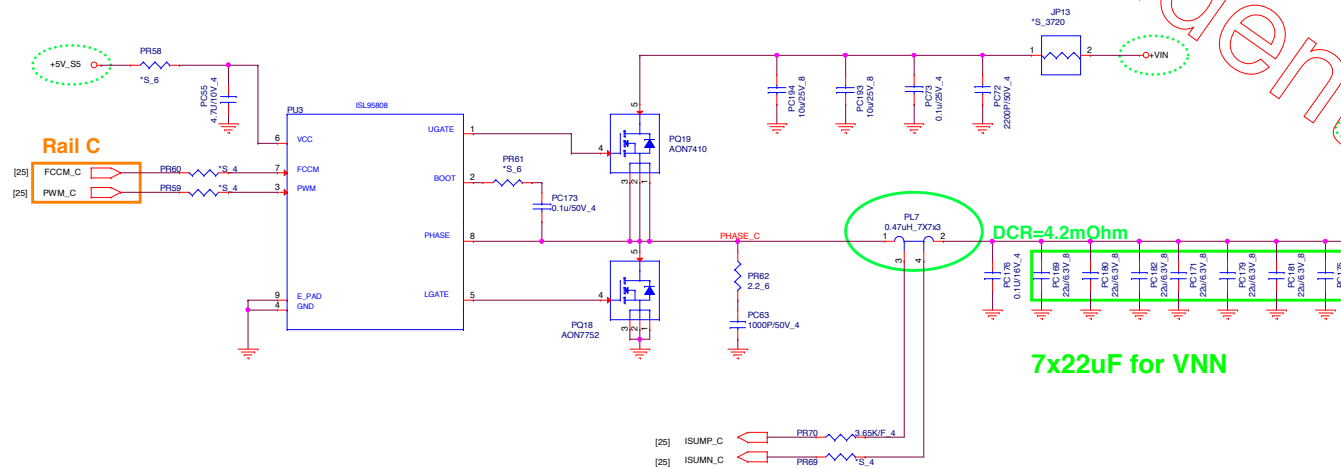


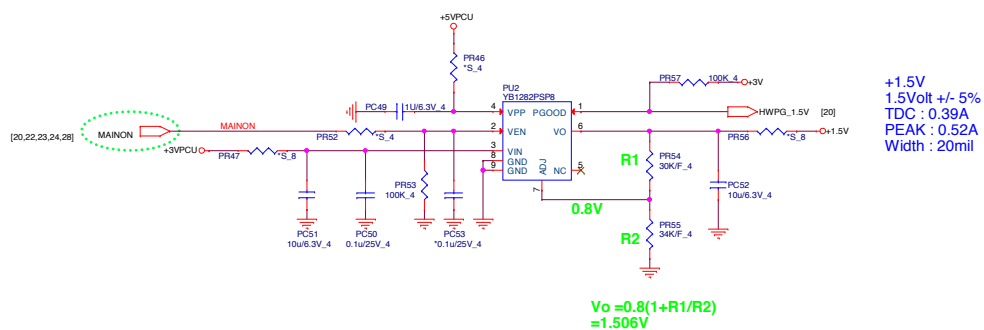
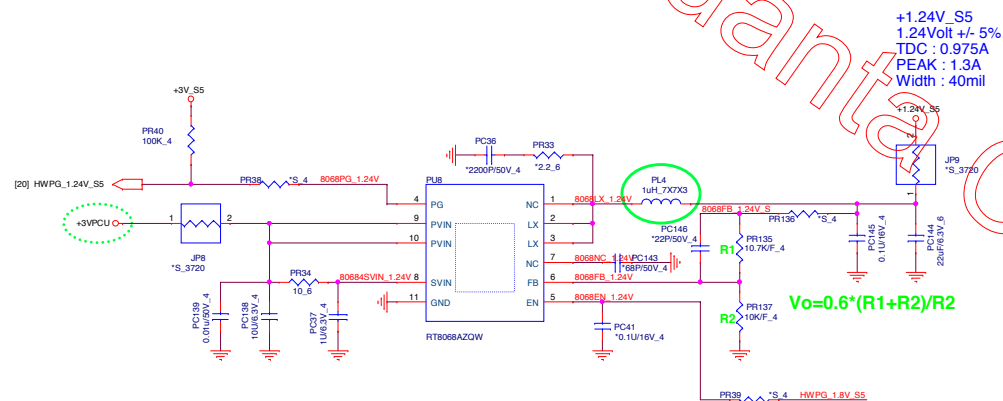
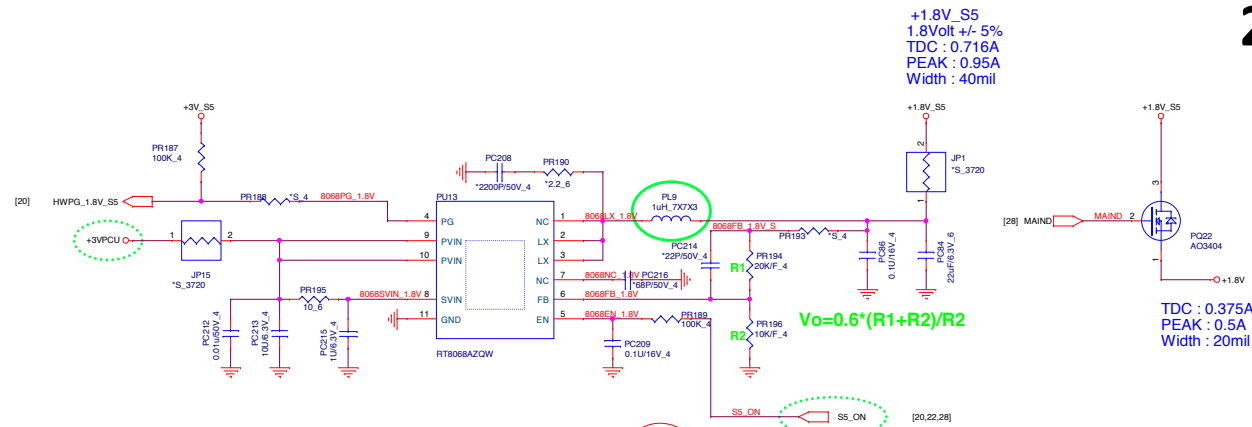
[12,16,21,22,24,25,28] +VIN
 [7,16,25] +VCC_VCCGI
 [7,16,25] +VNN
 [16,19,22,24,25] +5V_S5

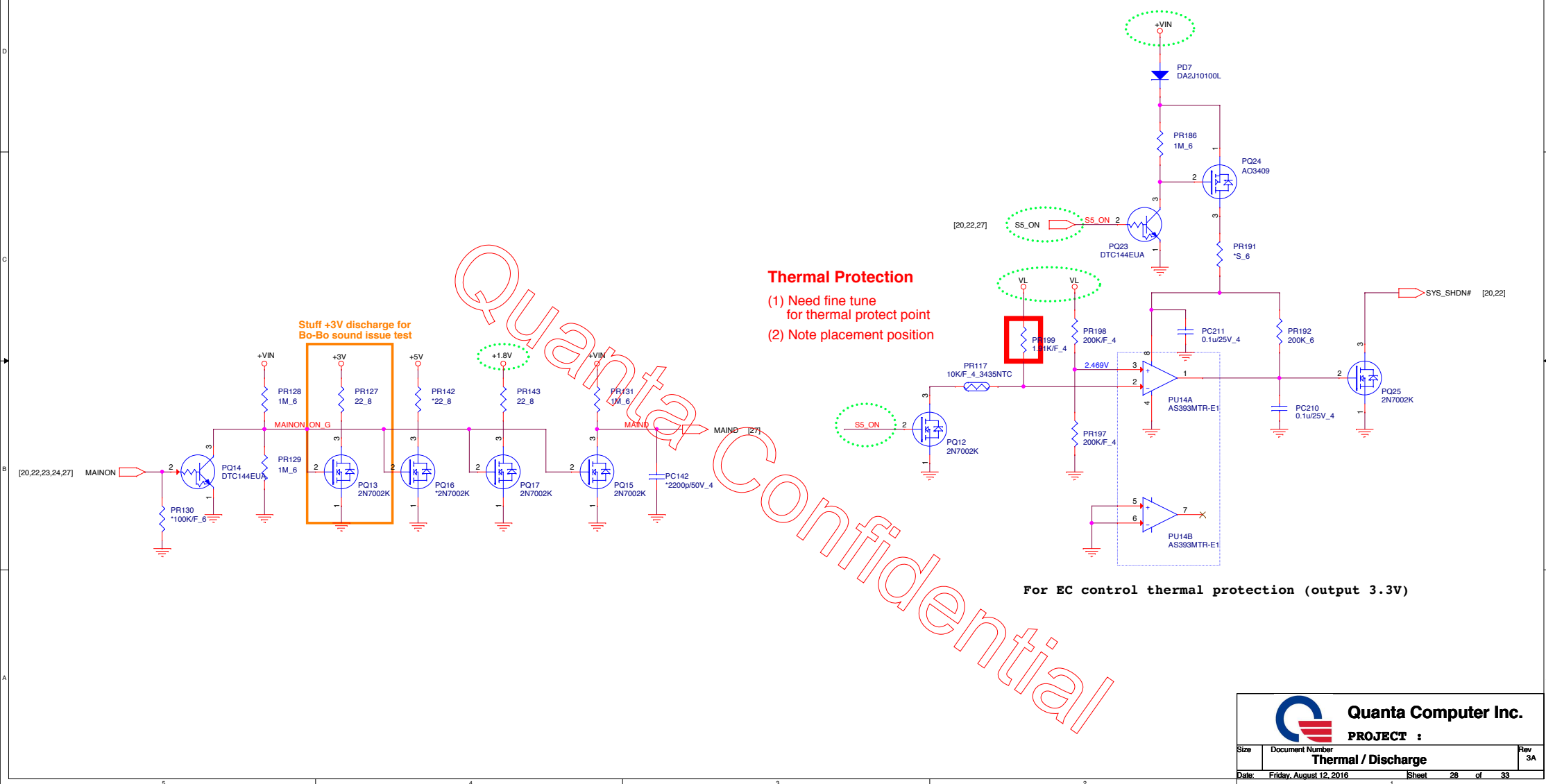
VCCGI



VNN







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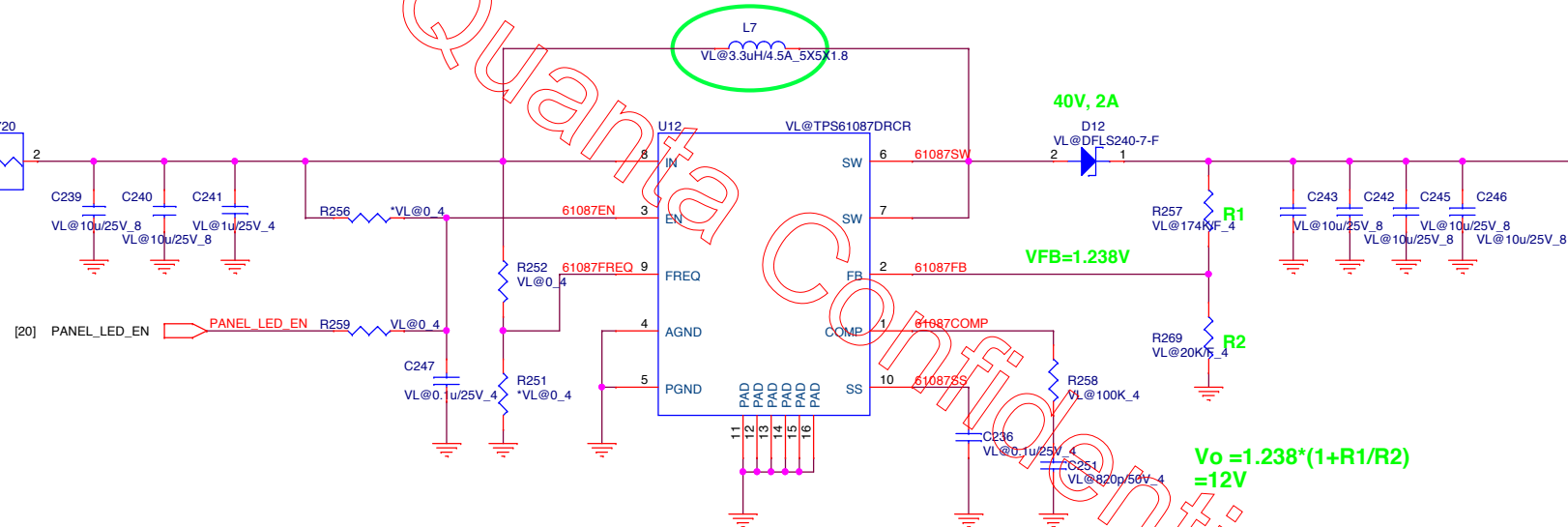
PROJECT :

Thermal / Discharge

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Panel Spec (TFT-LCD 14")
 VLED : 6V~21V (Tpy:12V)
 Power Consumption : 3W (MAX)

+12V_Panel
 12 Volt +/- 5%
 PEAK : 0.35A
 Width : 20mil

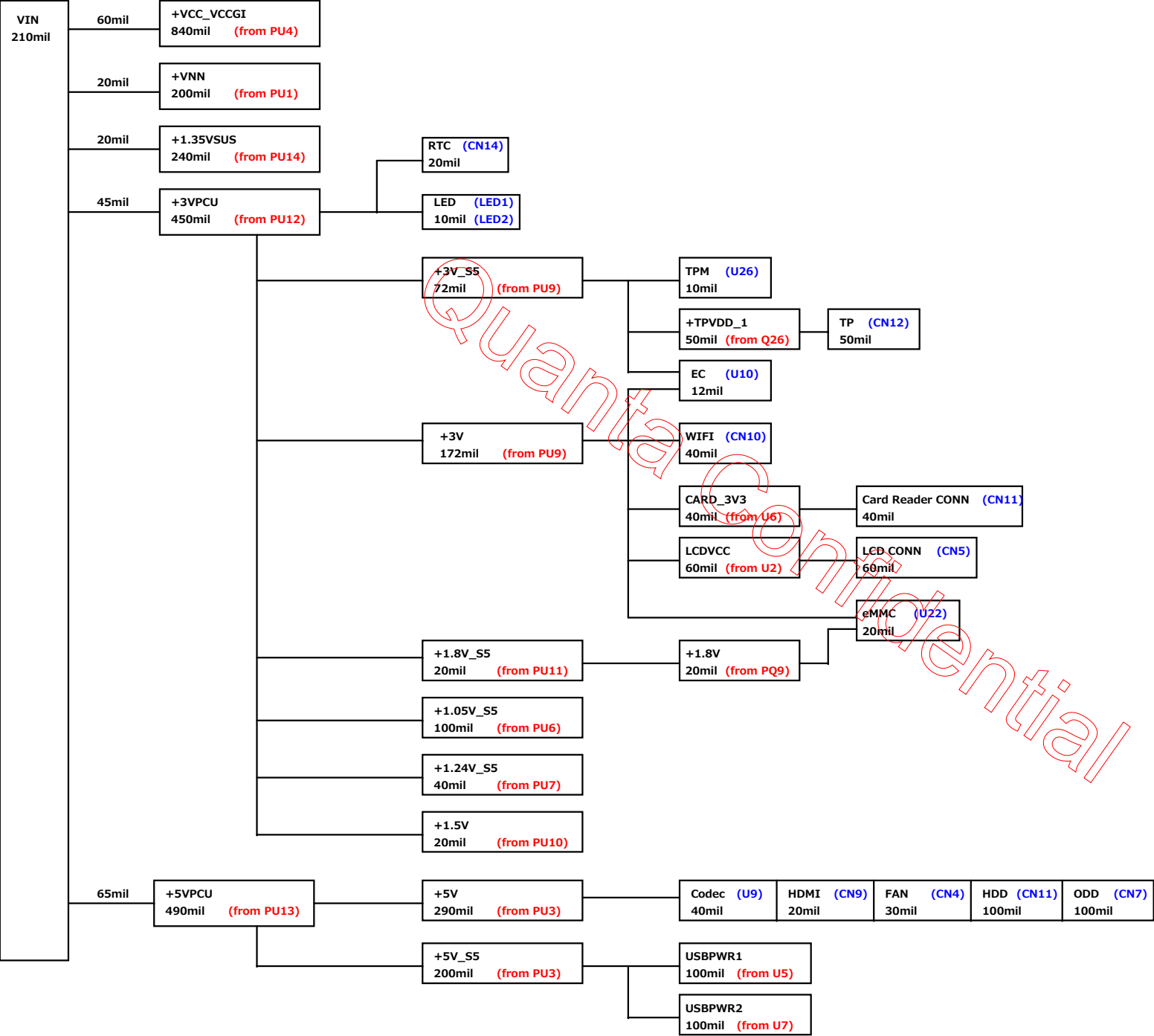


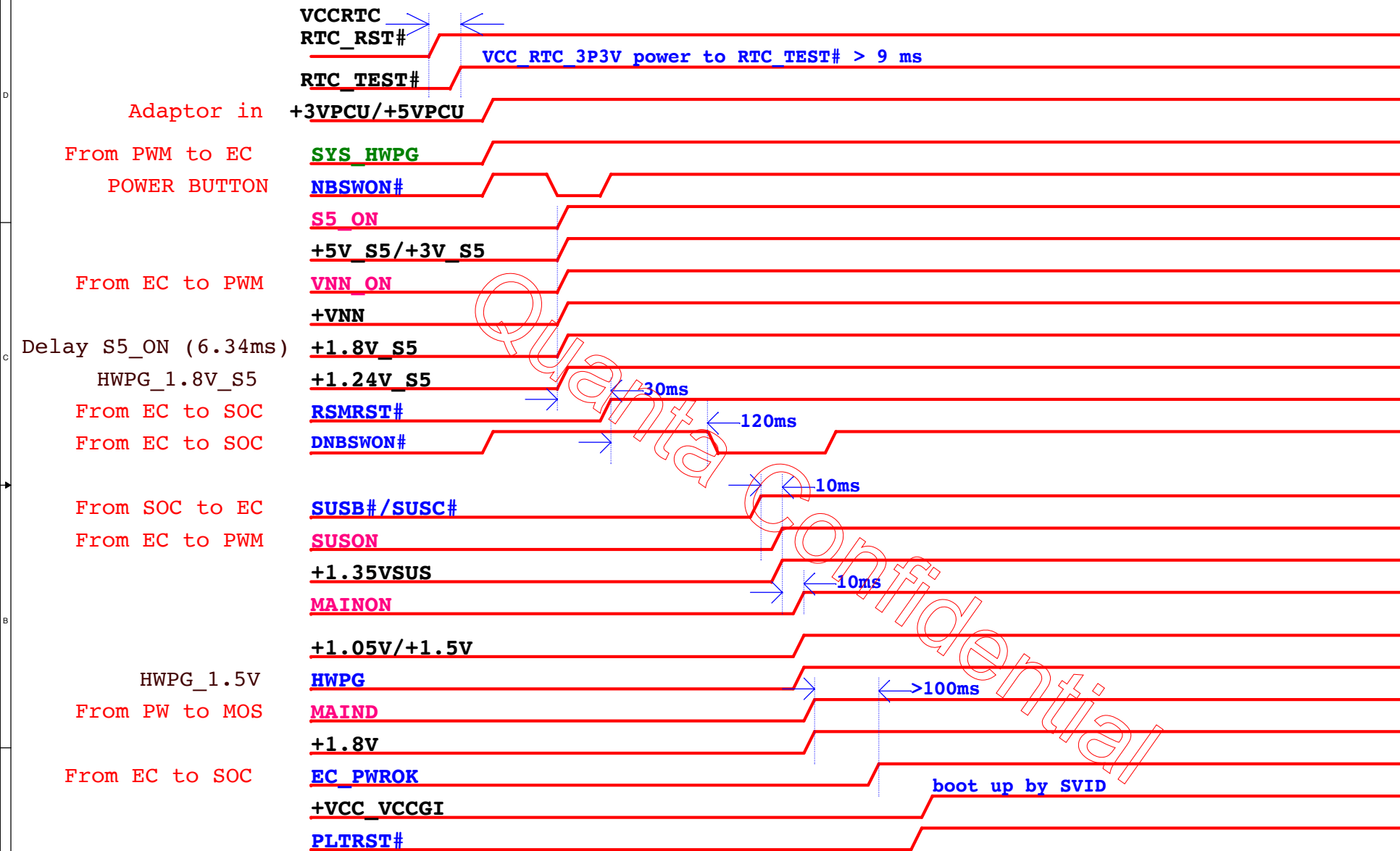
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PROJECT :

LED Panel (TPS61087)

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Power plane	Description	S0	S3	S5
+VIN	Adaptor power supply	ON	ON	ON
+VCC_VCCGI	Variable voltage supply to CPU and Graphics Core and ISP logic	ON	OFF	OFF
+VNN	Variable voltage supply to other (non core) logic	ON	OFF	OFF
+1.05V	Fixed voltage rail for SRAM,I/O,internal Logic	ON	OFF	OFF
+1.24V_S5	Fixed voltage rail for SoC L2/ Audio & ISH I/O Logic and PLLs MPHY Logic/ USB2-I/O/MIPI I/Os	ON	ON	ON
+1.8V_S5	Fixed voltage rail for all GPIOs	ON	ON	ON
+1.35VSUS	Fixed voltage rail for DDR3L IO	ON	ON	OFF
+3V_RTC	Fixed Voltage rail for RTC (Real Time Clock)	ON	ON	ON
+1.8V	1.8V S0 power rail	ON	OFF	OFF
+1.5V	1.5V S0 power rail	ON	OFF	OFF
+5VPCU	5V always on power rail	ON	ON	ON
+5V_S5	5V S5 power rail	ON	ON	ON
+5V	5V S0 power rail	ON	OFF	OFF
+3VPCU	3V always on power rail	ON	ON	ON
+3V_S5	3V S5 power rail	ON	ON	ON
+3V	3V S0 power rail	ON	OFF	OFF